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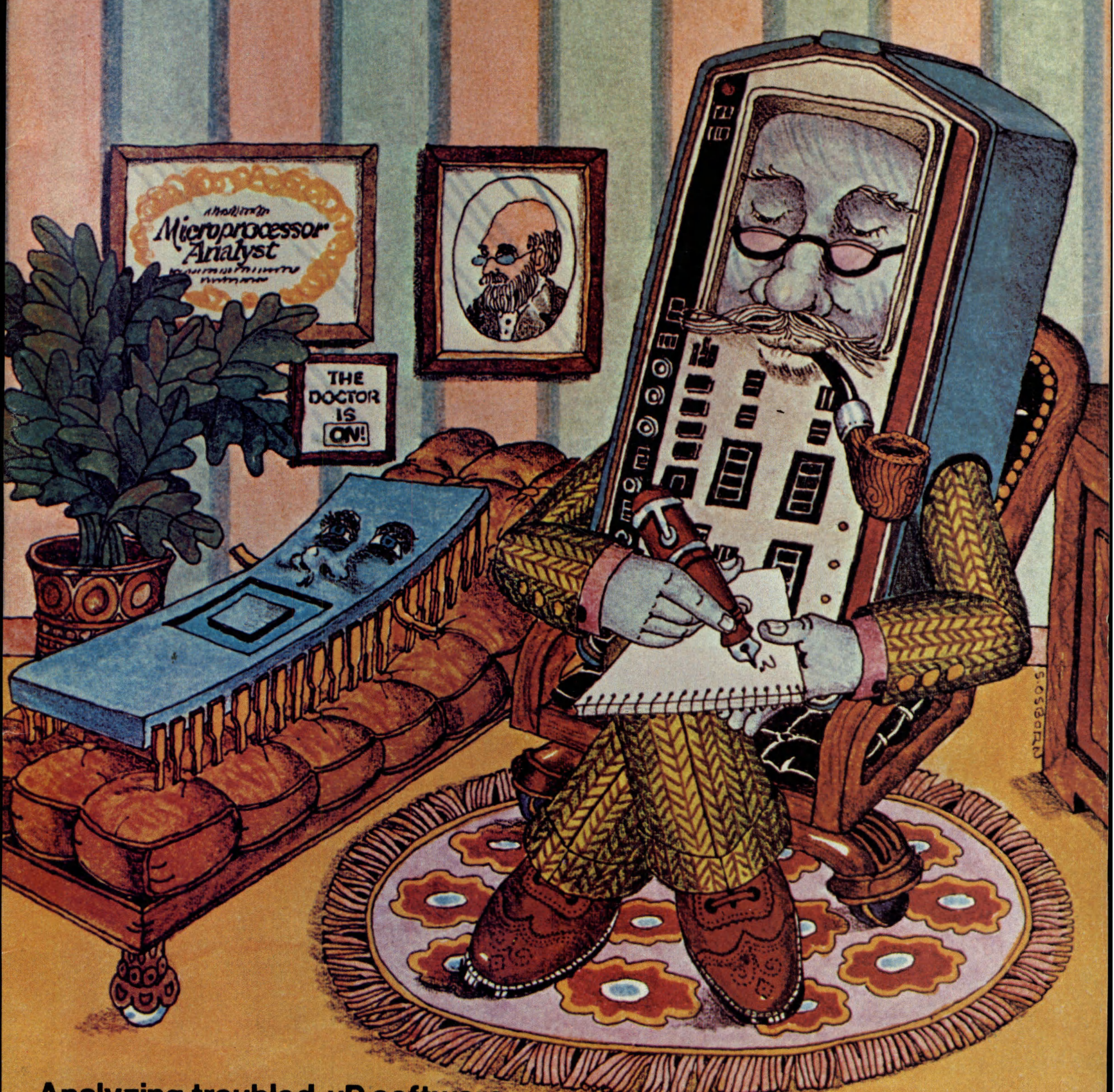
digital design

the magazine of digital systems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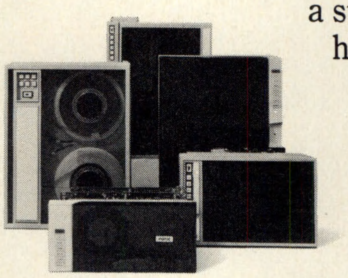

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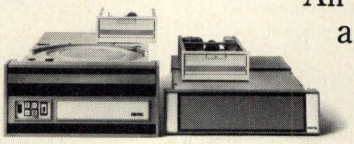

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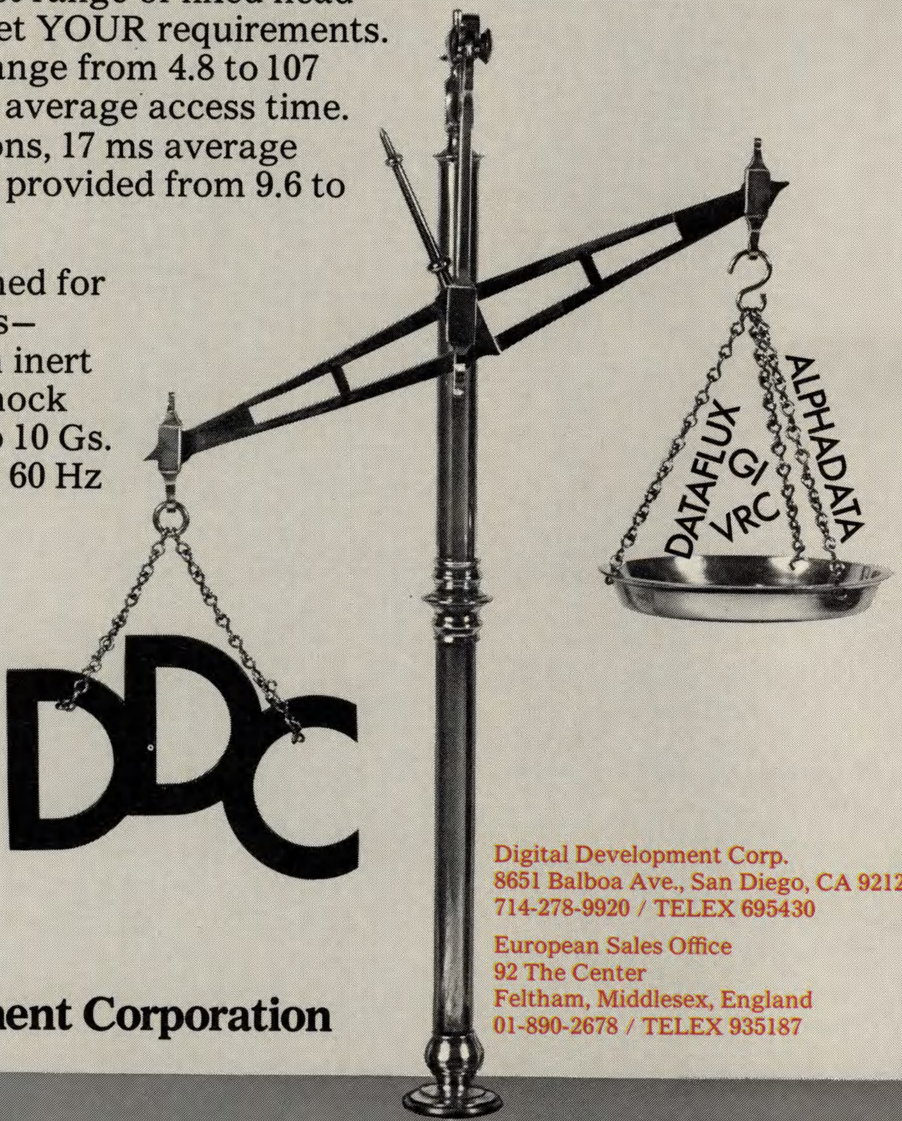

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CIRCLE 6

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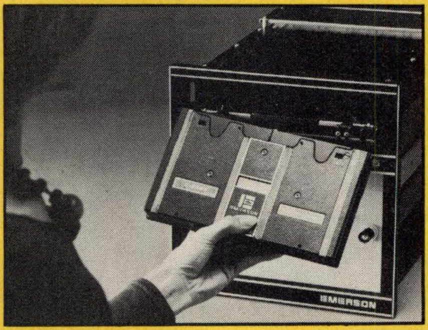
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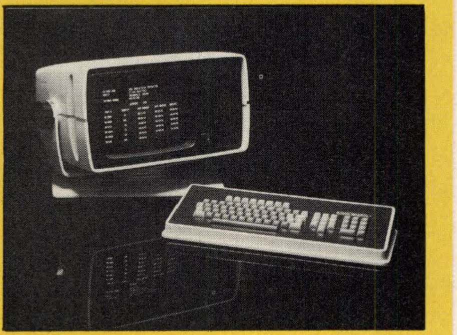
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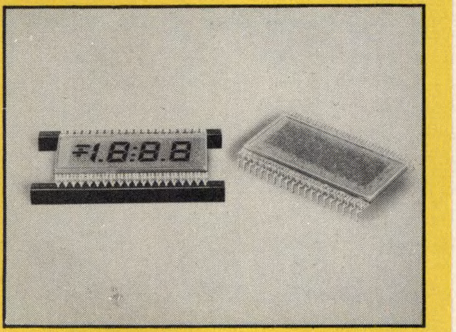
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You say your µP system's tongue-tied, weak on its pins, unresponsive? To find out how to avoid such problems, turn to part two of our microprocessor software series on page 48. And to find out how one µP-system "doctor" diagnoses such ills, turn to page 23. Cover art by Steve Osborn, courtesy Biomation. Cover design by Mary Ann Parker.

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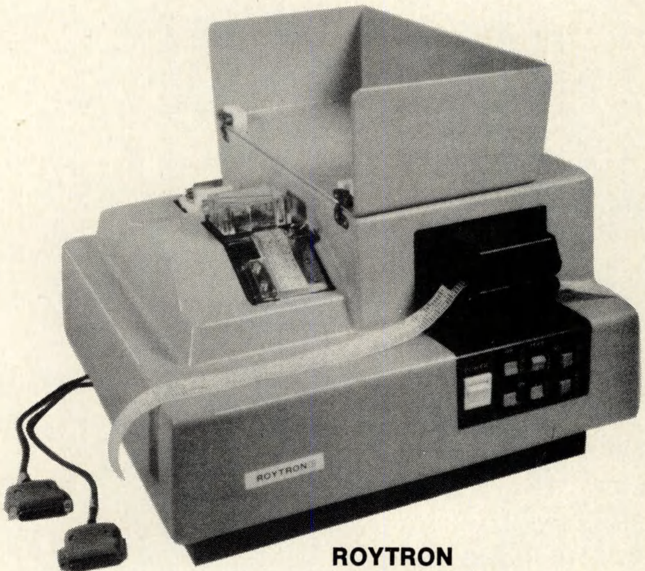
a plug for our quiet one



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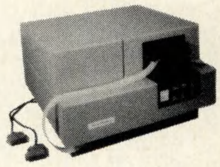

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CIRCLE 7

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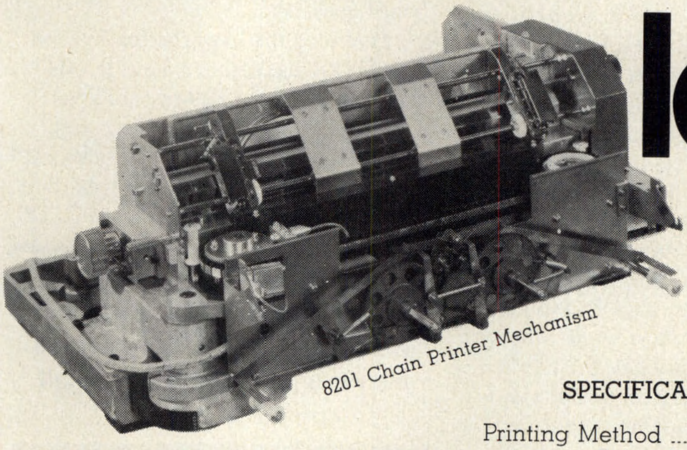

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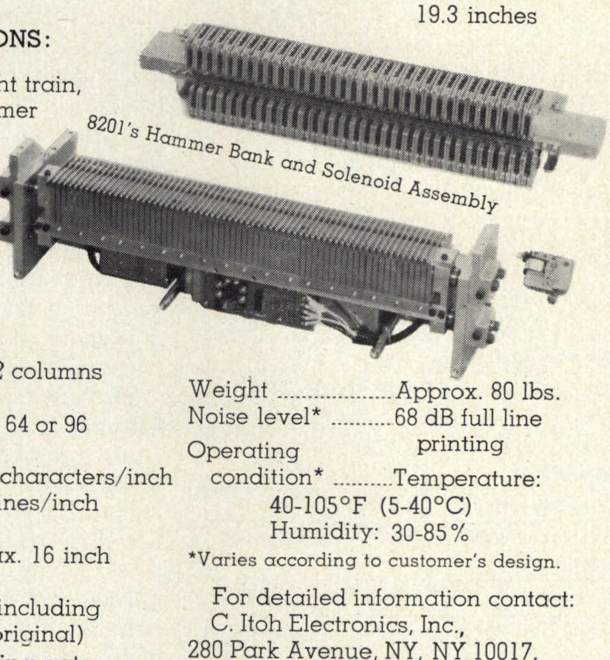
Number of characters	48, 64 or 96
Character spacing	10 characters/inch
Line spacing	6 lines/inch
Width of print paper	Max. 16 inch
Number of copies	6 (including original)
Paper loading	Swing gate
Paper feed*	One pair of pin feed tractors, 14 in./sec. (clutchless drive system)
Inked ribbon	1.18 inch W x 132 feet L
Inked ribbon feed	Special gear train
Frequency	50/60Hz ± 1Hz
Size (HxWxD)	11.3 x 24.8 x 19.3 inches
Weight	Approx. 80 lbs.
Noise level*	68 dB full line printing
Operating condition*	Temperature: 40-105°F (5-40°C) Humidity: 30-85%



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CIRCLE 8

technology trends

Cost, performance, reliability tradeoffs grow with increased memory-system use

The cost of semiconductor memory chips may continue to fall, but as computer performance increases, an increasing percentage of computer-system hardware – and thus computer-system cost – is dedicated to data storage. Consequently, say two memory-system designers, the tradeoffs between cost, performance and reliability in memory systems grow increasingly important to both designers and users of such systems.

Detailing these tradeoffs, Robert Koppel and Irwin Maltz, engineers at Intersil, Inc., note that optimizing memory-system organization means minimizing the number of peripheral circuits a system uses; the procedure cuts costs and increases reliability, though it may reduce operating speed.

But how do designers attain such minimum peripheral-circuit usage? Respectively manager of applications engineering and director of systems engineering at the Sunnyvale, CA, firm, Koppel and Maltz point out that techniques for achieving this goal vary with system size. Large, 32K x 18 storage cards can utilize on-card driver and sense circuits, but in such systems timing and control circuits are best consolidated so that one control card drives about four storage cards. The exact number of control cards depends on system speed requirements.

	4K RAM	8K RAM	16K RAM
Number of RAMs	64	32	16
Storage device cost	0.09	0.075	0.079
Storage device board cost	0.002	0.001	0.0005
Non-storage cost	0.043	0.019	0.011
System assy/test cost	0.025	0.013	0.007
Overhead	0.048	0.032	0.029
Total Cost	0.208	0.140	0.127

For a hypothetical 256K-bit semiconductor add-on memory system, the average cost to the system assembler, measured in cents/bit over the system's life, declines with increasing RAM capacity. Based on estimates of 1977 production figures, this breakdown assumes the assembler buys 16-pin, plastic-packaged RAMs produced on a 4" wafer; all intermediate costs are also given in cents/bit. ***(Source: R. Koppel and I. Maltz.)***

Smaller, 4K x 8 cards intended for microprocessor applications, on the other hand, incorporate their own control circuitry. The "grey area" occurs in systems that store about 16K bytes; some manufacturers of such systems offer on-card controllers while others provide separate units, say the two engineers, who reported on memory-system tradeoffs in September to Compcon 76.

"Dirty" power supplies affect performance. Chief among the factors that affect memory-system performance are electrostatic discharge and power supply noise and heat, according to Koppel and Maltz. Especially harmful in large systems, discharges can induce voltages in memory systems and the cabling that connects them to CPUs.

Damage in minicomputer systems often results from ripple generated by "dirty" power supplies. Such noise subtracts from memory-system thresholds at both address and data output pins. Spending "a few dollars" to reduce power supply output impedance and provide on-board filtering in such systems can provide dividends in the form of relaxed device specifications.

System cost depends on RAM size. Summarizing the cost considerations for a hypothetical 256K-bit card system, Koppel and Maltz note first that RAM costs form the primary component of total card system cost. RAM cost per bit declines predictably as RAM capacity increases from 1K to 8K, and 16K units cost only slightly more than 8K ones.

The cost per bit of such non-storage requirements as circuit boards and control circuitry also decreases as RAM capacity increases; for a given RAM capacity, cost per bit declines and then levels off with increasing total circuit board capacity.

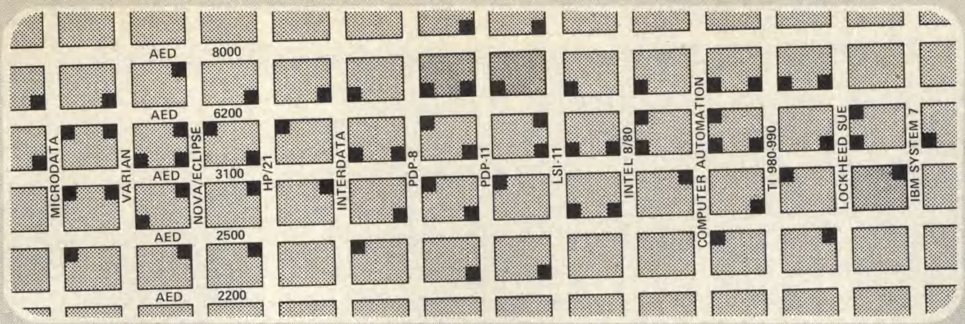
Assuming the hypothetical system uses plastic-packaged, 16-pin RAMs that allow 250- to 300-ns card-level access times and are produced on 4" wafers, the two engineers' system-cost summary *(see table)* shows a total cost per bit to the system supplier of 0.208 cents, if the system incorporates 4K RAMs. The figure drops to 0.127 cents if the system incorporates 16K RAMs.

Spending "a few dollars" on power supply filtering and impedance control can improve memory performance in small computer systems.

Error correcting codes increase system reliability. Examining the factors that affect system cost to users, Koppel and Maltz note that system reliability depends both on RAM performance and temperature effects, and that error correcting codes (ECCs) can increase system reliability, especially in large memory systems.

In a typical ECC implementation, a memory system receives input data and generates the ECC bits for it, then stores both the data and the ECC bits. Reading the data later, the system generates new ECC bits from it and compares them with the stored ECC bits; if the comparison checks out, no errors exist.

But ECC capability typically adds 40% more hardware to a memory system that stores 16-bit words, and its extra logic levels also add a 75-ns speed penalty in read access time. Still, as RAM cost per bit continues to decline 25% to 30% a year, the "insurance policy" provided by ECCs grows more popular in smaller systems, conclude Koppel and Maltz.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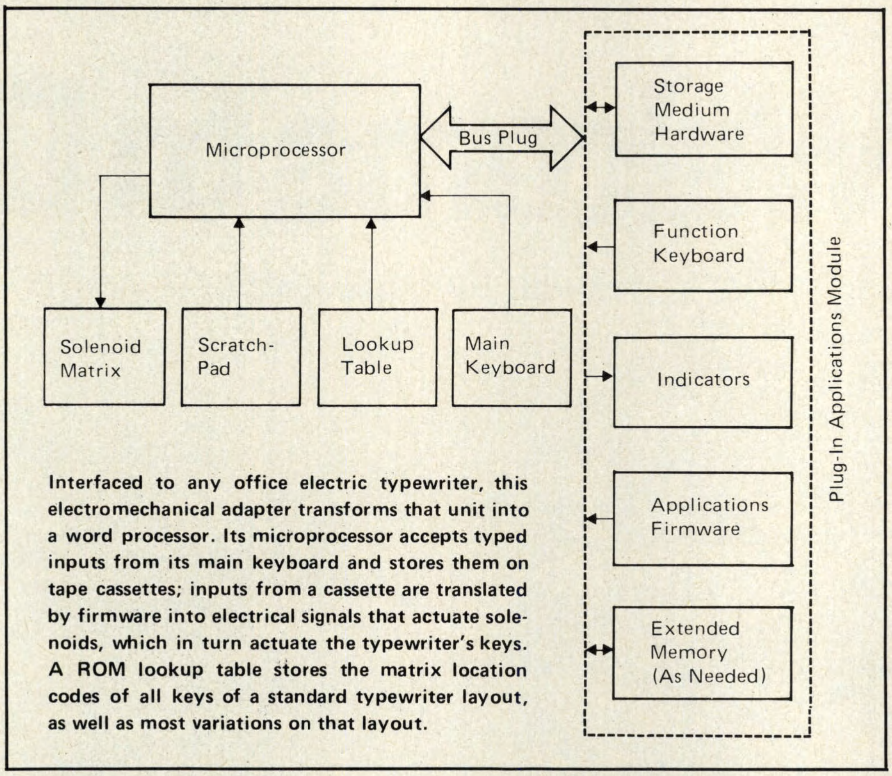
CIRCLE 10

Keyboard, solenoids transform typewriters into word processor systems

Attached to the keyboard of any type of office electric typewriter, an electromechanical interface transforms that typewriter into a word processor or dedicated data processor. Dubbed Type-Recorder, the prototype microprocessor based interface could cost less than $500 to produce in large quantities, says Mitchell Brody, a Brookline, MA, consultant and co-designer of the device.



Interfaced to any office electric typewriter, this electromechanical adapter transforms that unit into a word processor. Its microprocessor accepts typed inputs from its main keyboard and stores them on tape cassettes; inputs from a cassette are translated by firmware into electrical signals that actuate solenoids, which in turn actuate the typewriter's keys. A ROM lookup table stores the matrix location codes of all keys of a standard typewriter layout, as well as most variations on that layout.

Brody and Martin Stein developed the interface to meet what they perceive as a need for a low-cost, easy-to-use word processor that could serve specialized users – physicians, attorneys and small manufacturers, for example. To allow compatibility with typewriters other than IBM's Selectric, they designed the interface around a separate electronic input keyboard and a matrix of plunger-type solenoids.

Choosing solenoid types. Designed around an Intel 8008, the interface incorporates a scratchpad memory that allows the use of any typewriter keyboard arrangement without hardware modification. Firmware performs the code conversions required to translate the interface's keyboard inputs into signals to activate the solenoids; the firmware consults a ROM lookup table that contains the matrix location codes of all keys of a standard typewriter.

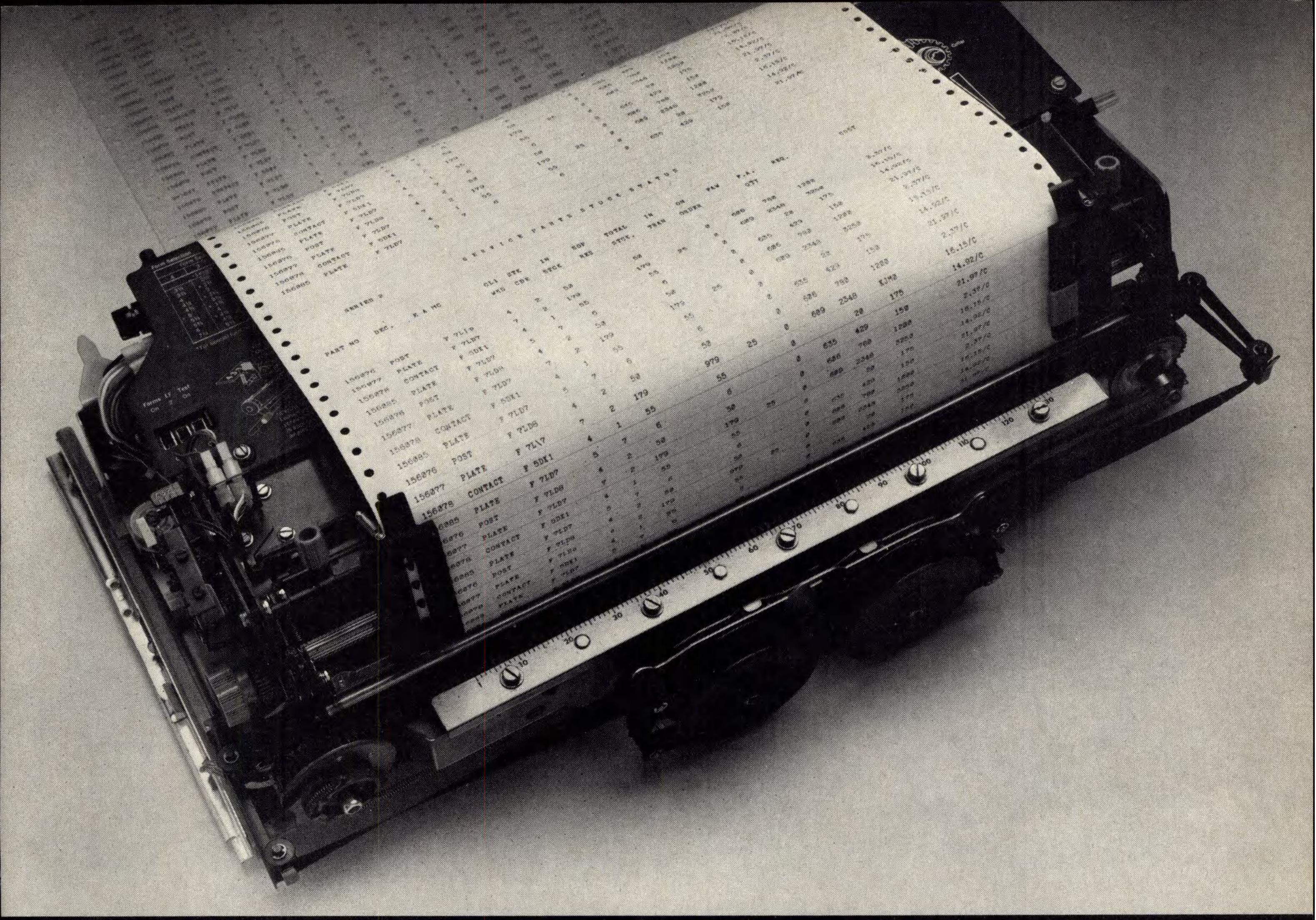
Brody recalls that the designers' primary effort focused on optimizing the solenoid matrix, whose units had to be small enough to fit in a dense array over a typewriter keyboard yet powerful enough to operate the keys even at the increased temperatures generated by prolonged use. The solenoids also had to have a stroke long enough to allow for variations in key operation.

Because of cost constraints, the designers rejected tubular solenoids – the most efficient type – and chose instead to use less efficient but cheaper frame-type units. The interface drives these solenoids in a short duty cycle at increased voltage levels, thereby eliminating the danger of overheating, according to Brody.

Popular keys get larger solenoids. Because some keys – space and underline, for example – experience heavy use, Brody and Stein located them on the periphery of the interface's keyboard and provided them with larger solenoids. Shift and shift lock keys also utilize heavier solenoids.

During output operations, the proprietary design's microprocessor acts as a dedicated controller of solenoid timing. It also governs shift operation, output speed and timing for the interface's tabulator and carriage return; it can adjust operation to accommodate typebar machines as well as faster, single-element typewriters.

CIRCLE 11▶



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micro notes

Designing a multi-µP-based computer family

Even as microprocessors appear singly in an increasing variety of industrial, scientific and consumer products, designers have begun contemplating the techniques and strategies required to implement multi-microprocessor systems. One consultant's study has revealed that a 10,000-node network of microcomputers could by 1985 function 40 times as cost-effectively as the most advanced large computer then available *(Digital Design*, February, page 26). Some multi-µP-based terminals and other peripherals have already reached the market; no doubt many more systems will debut soon.

What considerations arise in the design of such multi-microprocessor systems? What tradeoffs must the systems' designers face? Addressing such questions, Digital Systems Corp. engineering VP **Robert Laughlin** briefed Compcon 76 on the design of the Walkersville, MD, firm's Galaxy/5 family of computers, each of which incorporates from 10 to 60 microcomputers. Herewith, his report:

The design of any computing system involves the tradeoff of competing requirements. The speed with which individual instructions are executed represents only one such requirement, and the Galaxy/5 family of computers is not, nor was it intended to be, the fastest or most powerful computer in its class. In addition to raw execution speed, other design considerations are important, including:

★ Adaptability to change
★ Reliability and maintainability
★ Total system (not just CPU) price
★ Application throughput speed
★ Compatibility within the complete family.

To meet these criteria, we first separated our computing system into basic components; of these, all but the memory elements appeared likely candidates for microcomputers. But because this initial system doesn't allow for sufficient device overlap, we added additional elements of each type to the design (Fig 1); in the modified system, the memory is interweaved, the processors are close-coupled and the I/0 is separated into groups.

Such a system can achieve much greater concurrency than is possible with conventional computers. Each of the memory stacks can separately respond to cycle requests from the individual processors and the I/0 controllers. Each of the processors can execute a separate instruction stream at the macro level while the I/0 controllers respond to the data needs of the external devices.

The complexity of the interconnections depicted in Fig 1 require adding an additional, fifth circuit element to the system components. In the final system (Fig 2) this circuit element – the priority cross connect – is used in two separate areas. First, it "fans out" the memory stacks for connection of up to four processors and four DMAs; second, it connects the four processors to the stacks of DMAs.

Design ground rules. To ensure that the system would work when all of the individual elements were connected together, we established many design rules, including:

★ The system operates in an asynchronous environment; each element has its own clock. Our designers suspected that faster microcircuits will appear in the near future, but that these speed improvements will occur in non-uniform increments. Separate clocking allows greater flexibility as these new circuits become available.

★ Each element of the system is self-contained, if possible, on a single circuit card. Redesign of elements to take advantage of new microcircuits is thus

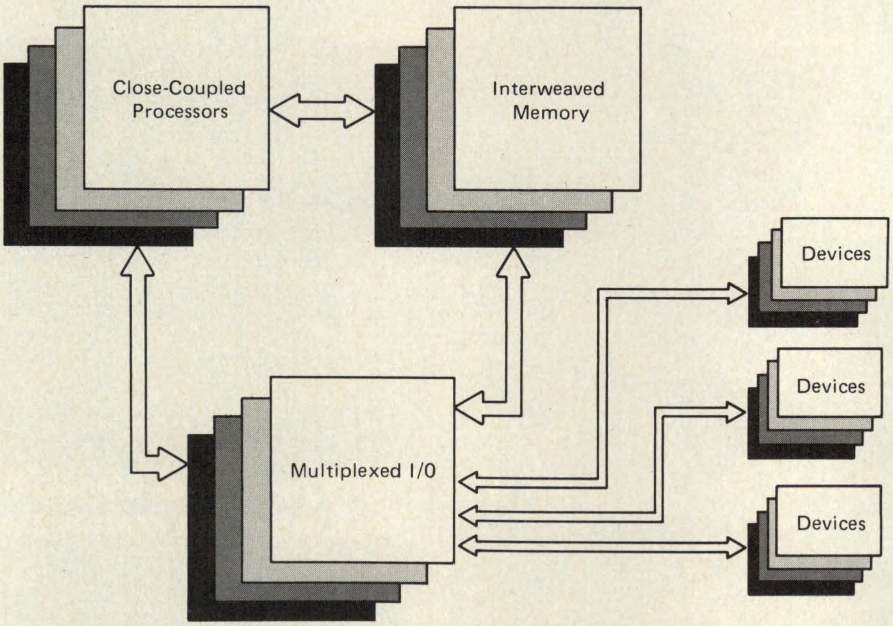

Fig 1 To allow for device overlap, the designers modified the basic system by adding additional basic components. They interweaved the memory elements, close-coupled the processors and separated the I/0 into groups.

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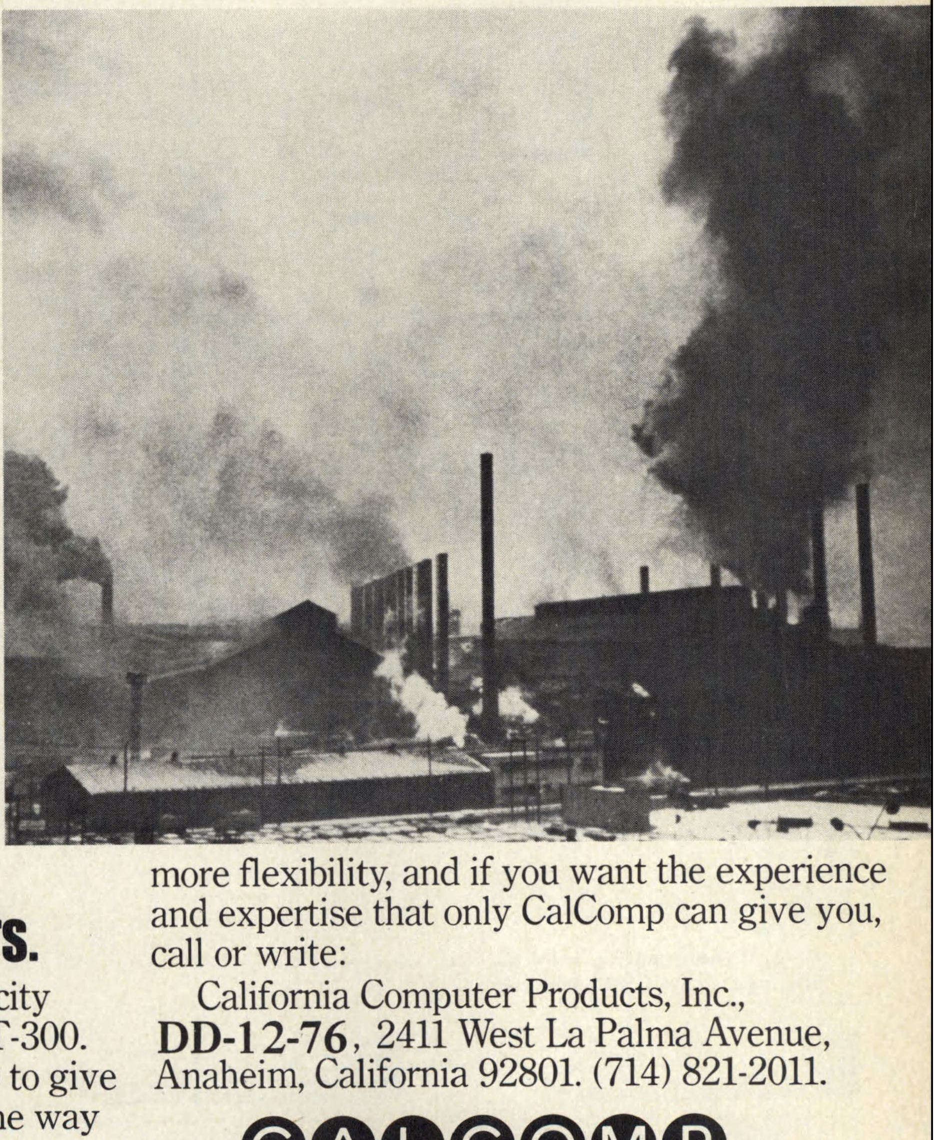

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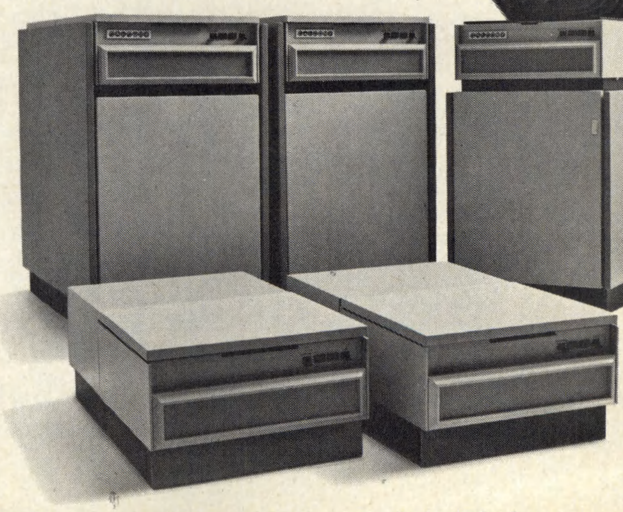

CIRCLE 13

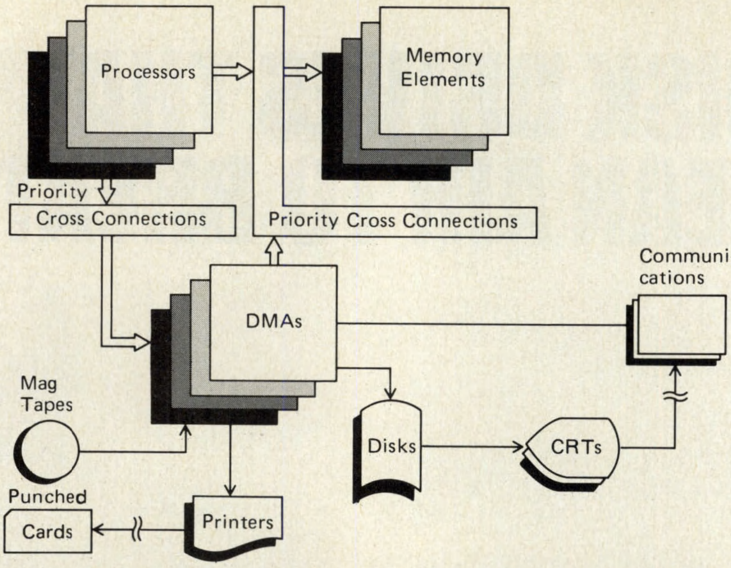
Processors
Memory Elements
Priority
Cross Connections
Priority Cross Connections
Communications
DMAs
Mag Tapes
Disks
CRTs
Punched Cards
Printers

Fig 2 Final system configuration incorporates a priority cross connect, which both fans out memory stacks for multi-processor and DMA connection and connects processors to DMA.

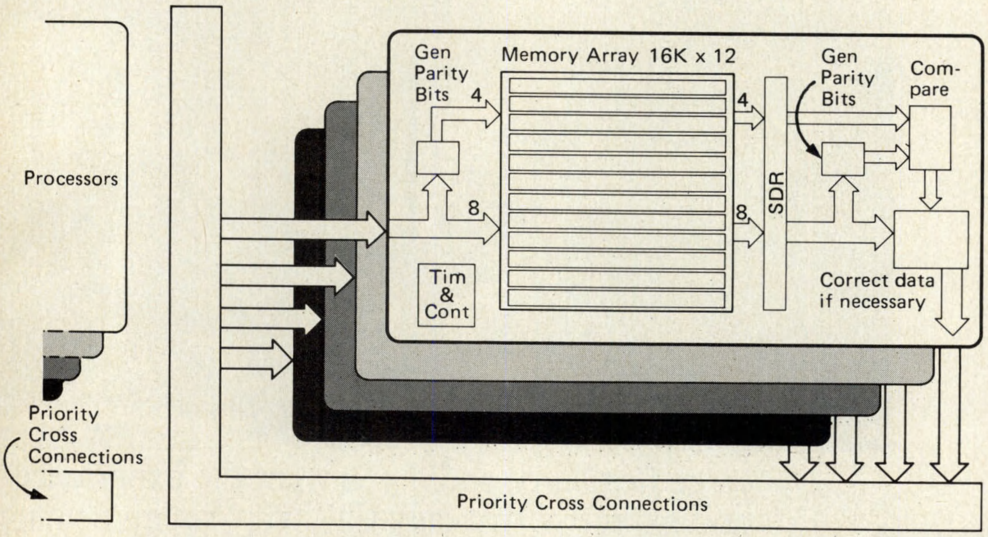
Processors
Priority Cross Connections
Gen Parity Bits
Memory Array 16K x 12
Gen Parity Bits
Compare
4
8
4
8
SDR
Tim & Cont
Correct data if necessary
Priority Cross Connections

Fig 3 In main memory, individual stacks are unaware of each other, and priority cross connect logic handles stack number decode.

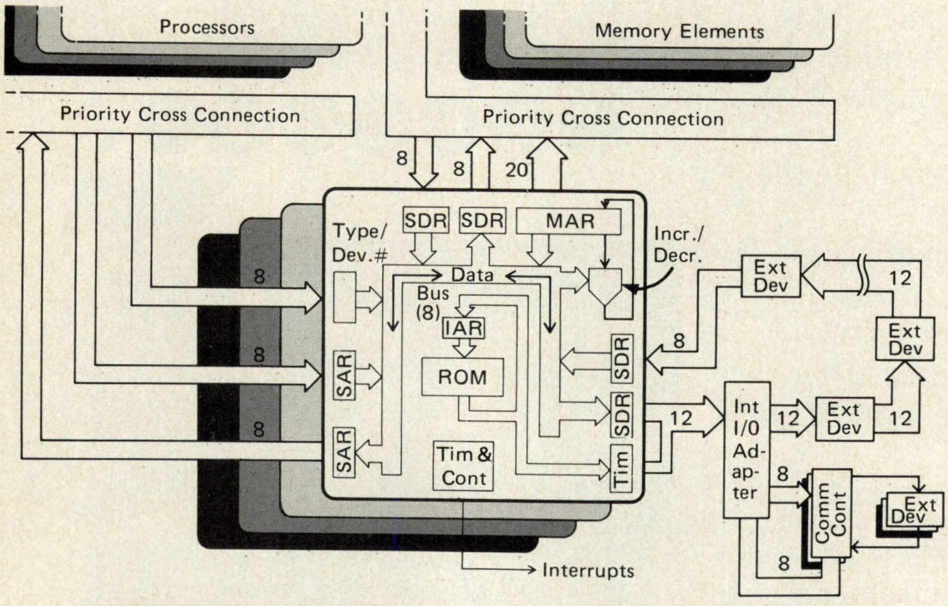
Processors
Memory Elements
Priority Cross Connection
Priority Cross Connection
8
8
20
Type/ Dev.#
SDR
SDR
MAR
Incr./ Decr.
Data
Bus (8)
IAR
ROM
SAR
SAR
SDR
SDR
Tim
Tim & Cont
8
8
8
Ext Dev
12
Ext Dev
8
12
Int I/0 Adapter
12
Ext Dev
12
8
Comm Cont
Ext Dev
8
Interrupts

Fig 4 DMA controller maintains a memory address register for each device connected to it by a 12-wire loop — a connection scheme that mandates byte-multiplexed transfers.

simple, because up to now, each of the "one-chip" microprocessors requires five or more unique support chips.

★ Standard interfaces, designed as narrowly as practical, connect the various elements together. These interfaces should remain constant despite the anticipated redesign of individual elements.

Microprocessor selection. Other proposed multi-microprocessor systems are composed of various numbers (often quite large) of microprocessors, all of the same type. Such a design has some advantages, particularly part-number reduction, but the disadvantages of using a single processor type for a wide range of requirements appear too great to adopt this technique as a general-purpose solution for a large-scale computer system.

Cycle time was the most important factor in our selection of microprocessors. In the communications controller, the slow data rates (9600 baud in the asynchronous mode and 24,000 baud in the synchronous mode) permit the use of any available eight-bit microprocessor.

For the main processor elements, we deemed 375-ns cycle time adequate and therefore chose a "bit-sliced" microprocessor. In the disk controller the data rates reach one million bytes/second, which is beyond the reach of any currently available microprocessor. Therefore, we designed a special-purpose microprocessor for this task.

Prior to the Galaxy/5's design freeze, we considered many alternative configurations. One method of achieving concurrency that has received much attention involves overlapping operations within one instruction stream. This method was first used on a hardwired machine — the IBM 360/91 — but in a microprocessor based machine tremendous overhead is generated in status checking and coordinating activities, and the interconnections between elements become wider.

Main memory (Fig 3) uses 4K RAM dynamic chips. Because Galaxy/5's memory holds up to one million bytes, we felt it necessary to design in single-bit error correction codes. Consistent with our philosophy of element independence, individual memory stacks are not aware of each other's existence. Stack number decode is handled by the priority cross connect logic.

I/0 configuration. In each of the computers' special-purpose I/0 elements, a microcomputer controls but does not directly participate in data movement. Most data transfers occur

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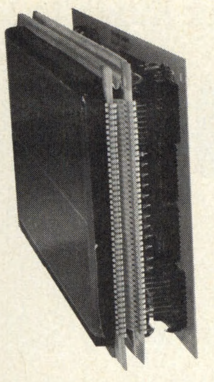

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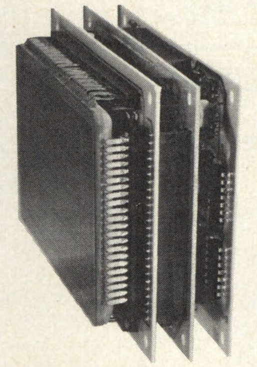

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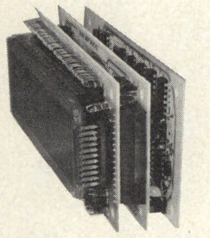
"Maxi-64"



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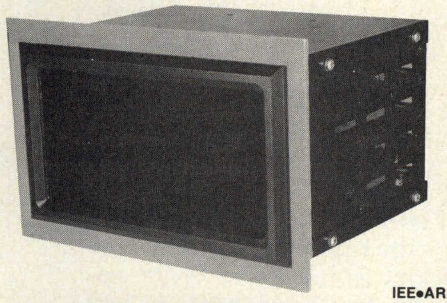
"Maxi-32"



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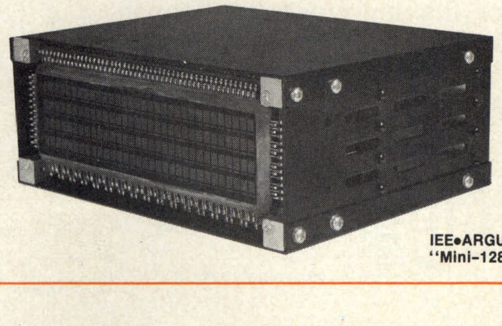

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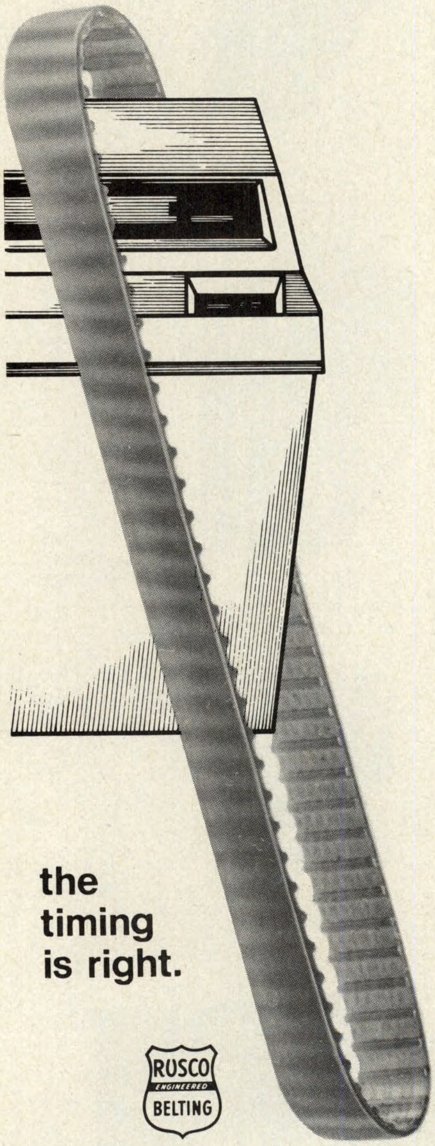
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CIRCLE 15

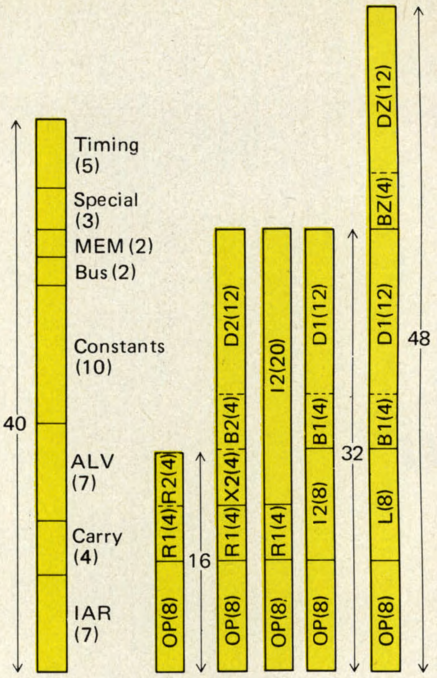
Timing (5)
Special (3)
MEM (2)
Bus (2)
Constants (10)
ALV (7)
Carry (4)
IAR (7)
40
OP(8)
R1(4)
R2(4)
16
OP(8)
R1(4)
X2(4)
B2(4)
D2(12)
OP(8)
R1(4)
I2(20)
OP(8)
I2(8)
B1(4)
D1(12)
32
OP(8)
L(8)
B1(4)
D1(12)
BZ(4)
DZ(12)
48

Fig 5 Micro instruction format (left) assigns a fixed meaning to each bit. Macro instruction formats used in the computer (five of seven possible formats are shown) have three different lengths. They increase the power of the computer's instruction set (which consists of 108 instructions) without correspondingly raising hardware cost.

from memory to device or device to memory. However, programmed data transfers (main processor to device and device to main processor) are available. The direct memory access (DMA) controller (Fig 4) maintains a memory address register for each device connected to it.

Connection to external devices occurs through a standard twelve-wire loop, whose design eliminates the need for either additional lines to each device (star configuration) or the use of bidirectional bus drivers (daisy chain). But this design does necessitate byte-multiplexed transfers.

Here is a typical sequence of events during an I/0 operation:

★ The application program requests the I/0 operation from the supervisor program.

★ The supervisor places the application program in the Wait state and checks the validity of the request.

★ The supervisor executes a Load I/0 instruction, which transfers the buffer address to the memory address register within the DMA.

★ The supervisor executes a Command instruction, which sends an eight-bit command code to the appropriate device via the DMA.

★ The main processor then proceeds with other work. The supervisor passes control to another application program if one is in the Ready state.

★ The device requests data cycles from the DMA at a speed dependent on its internal timing. The DMA prioritizes the requests and honors them when it can.

★ The device ends its operation, either because of error or normal completion, and requests an interrupt cycle.

★ The DMA prioritizes the interrupt requests and signals the processor.

★ The processor interrupts its operation to service the interrupt request and marks the original application program Ready.

The I/0 configuration was actually the first set of elements designed. Our engineers felt that in our market (commercial timeshare), I/0 capability

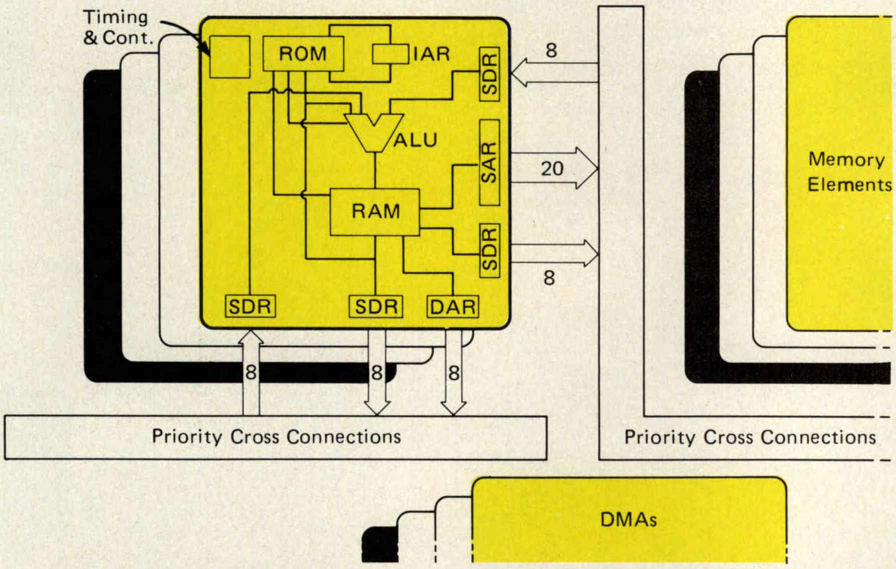
Timing & Cont.
ROM
IAR
SDR
ALU
SAR
RAM
SDR
SDR
SDR
DAR
8
20
8
8
8
8
Memory Elements
Priority Cross Connections
Priority Cross Connections
DMAs

Fig 6 Main processor hardware executes macro codes by acquiring operands from memory or registers and placing results in either memory or registers, depending on the instruction. Each processor contains index/base registers and a parallel arithmetic logic unit (ALU).

would tend to form the limiting factor on throughput. After all, enormous computer power is of little value if you can't get the questions in or the answers out.

Close-coupling the processors. Each Galaxy/5 system consists of one to four main processors, connected in a configuration termed "close-coupled." In this configuration, a processor element is simply a resource, just like an area of memory.

A program requests the use of a processor by being in the Ready state. The processors are all equivalent so far as the program is concerned, and any one of them might be assigned to execute a segment of an application program. Later, another processor might be assigned to process another segment of the same program. No processor has a special relationship with main memory, and each processor can address all positions of main memory. Similarly, each processor can send commands to all of the attached external devices.

Why do we use one computer to emulate another, a procedure that is actually the essence of microprogramming? Certainly, emulation does result in slower execution speeds than are available with either a hardwired unit or a unit that places the macro instructions in main memory. But mere execution of instructions is not the goal of a computer system. Rather, the computer's goal is the accomplishment of an application expressed in instruction form for the convenience of the hardware. (Few programmers find machine code particularly convenient!)

To accommodate expected microcircuit speed increases, the designers used separate clocking circuits for each of the computer's elements.

In our choice of macro instruction formats, the paramount consideration was that they provide for the exact and precise expression of the solutions. Having chosen a macro format, we then attempted to find an efficient way of executing it. The greatest advantage of microprogramming is the increased power of the resulting instruction set, which occurs without a corresponding increase in the cost of the hardware.

Fig 5 shows a comparison of the micro and macro instruction formats.

Cont'd p. 20

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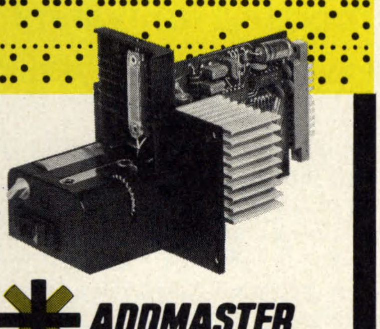

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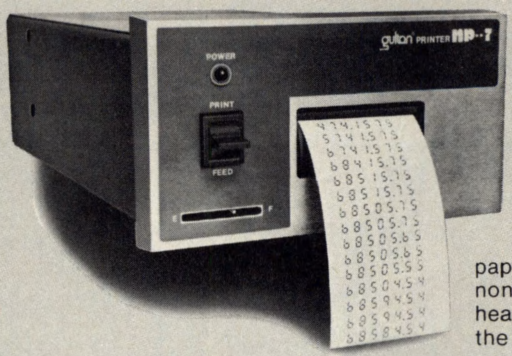

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CIRCLE 17

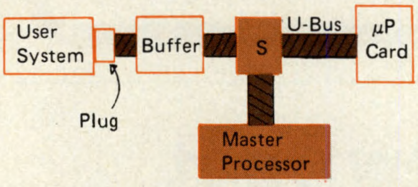
The micro instruction has a single fixed format in which each bit has essentially one meaning. The macro instruction has seven formats (five of which appear in Fig 5) with three different lengths. Individual bit significance varies considerably; the complete set has 108 instructions.

In the main processor hardware configuration used to execute the macro code (Fig 6), operands come from either memory or registers, and results can be placed in either memory or registers, depending on the individual instruction. Each processor contains its own set of index/base registers, and each contains a parallel arithmetic logic unit (ALU).

To increase performance within the product line, we can add up to three additional main processors to a standard one-processor system; each of these processors acts relatively independently of the other processors.

Proposed 'universal' in-circuit emulator serves any µP system, saves time and money

To serve designers who may utilize several different microprocessors in their projects, one manufacturer of microprocessor support hardware has proposed developing a "universal" in-circuit emulation system. Designed to implement a control scheme termed bus intercept, the system would allow a designer to use the same text editor, assembler, operating system and debugging package to analyze and troubleshoot any system designed around any current or contemplated micro.



Proposed in-circuit emulation system would utilize a master processor — either a mini or a micro — to execute an editor, assembler, debugger and file storage. The processor would execute emulation instructions after gaining control of the emulated system through a bus intercept controller (S).

Roger Doering, vice president at Digital Electronics Corp., Oakland, CA, explains that using an in-circuit emulation system lets a designer monitor a microprocessor system's activity, control that activity at any point in its programming and substitute a program stored in external RAM for any section of memory in the emulated system. A universal emulator would allow such operation for systems designed around any microprocessor without requiring extensive hardware changes to accommodate new chips.

By contrast, currently available in-circuit emulation systems can each serve one type of microprocessor, or at best one family of one manufacturer's microprocessors. Designers who desire to use more than one variety of microprocessor to optimize different applications must thus spend large sums on several different emulation systems and must also devote large amounts of time to learning how to use those systems.

Master and slave. Doering's proposed emulation system consists of a master computer — either a mini or a micro — and a slave microprocessor equipped with special control and monitoring hardware and with a memory imaging RAM. The master computer executes the emulator's editor, assembler, debugger and file storage, thereby requiring no software changes when a user switches to a different microprocessor system. This hardware independence permits implementation of the bus intercept control scheme, as well as making the full address space of the slave available to the user.

Utilizing a universal bus — 16-bit address and data buses and a control bus that allows such operations as 4-phase clocks — the slave system incorporates a sorting matrix personality card for emulated microprocessor. The card adapts a microprocessor's pinout configuration to match the emulator's structure.

Bus intercept design. In Doering's proposed system, which he described at Wescon, the master processor would intercept the slave's universal bus this way:

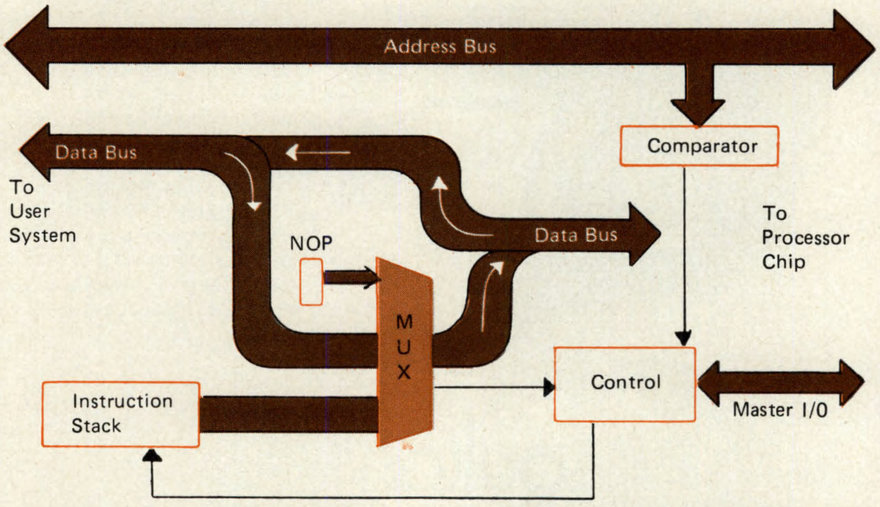
★ Comparator circuits — possibly associative memory — detect events defined and transmitted by the master.

★ The system achieves the synchronization required to attain the slave's next instruction.

★ A multiplexer feeds instructions, and associated control bits, from the interceptor's stack to the slave, which executes them regardless of the value of its internal program counter.

★ When the stack is exhausted, the multiplexer either feeds "no operation" instructions to the slave (either because the master wishes to idle the slave or because the master requires additional control time) or returns control to the slave's data bus. In the second case, slave execution commences from the current program counter value.

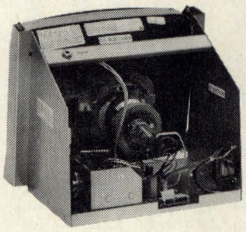
Doering also contemplates monitoring and memory imaging hardware to serve this bus intercept control scheme. Located on the universal bus between the interceptor and the user system, the memory imaging hardware would capture information from the buses in a circular stack, and the master would then review, display or analyze this information as required. Any special programming required to perform these activities would reside in the master's mass storage.



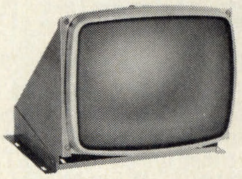
Simplified bus intercept controller contains a multiplexer (MUX) that feeds instructions from a stack to the emulator's slave microprocessor under control of the emulator's master processor. After all instructions are executed, control returns to the slave, either immediately or, if more time is required, after the slave executes several "no operation" (NOP) instructions.

If you make top-quality data terminals, here are four reasons to use Setchell Carlson CRT display modules in your system.

Reliability: Our data displays are outstanding solid-state designs with critically matched magnetics to optimize the performance levels and dependability demanded by your customers. We use the most advanced engineering and production techniques to assure consistency of performance. No data display is built with more deliberate attention to quality and reliability.



Delivery: We have been in the display electronics business long enough to know about rush orders. If you need it yesterday — we'll try to get it to you yesterday.



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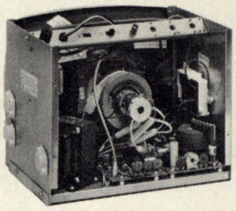

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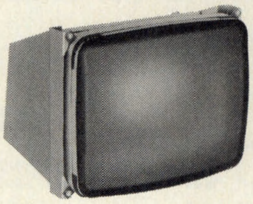

But don't take our word. See for yourself by contacting us today.

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CIRCLE 18

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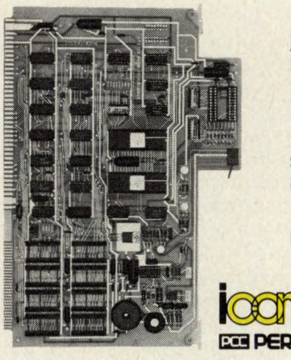

Now you can program 2708's & 2704's in just 100 seconds including automatic verify using iCOM's PROM Programmer/Memory Expander which occupies a single card slot in either Intel's* SBC 80/10 or Intellec* MDS-800. The PP80 card also provides sockets for 8 additional 2708/2704 type devices for memory expansion.

Just $395 including 1K ROM resident programming firmware.

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CIRCLE 19

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CIRCLE 20

Study urges standards for Navy µP systems

Microprocessors aren't just super-flexible system building blocks; effectively using them in military systems requires considering such additional factors as software, hardware maintenance, training and logistics. And lack of standardization in these areas has so far limited the use of microprocessors in military designs, say two staff members at the Naval Electronics Laboratory Center.

To solve this problem, the San Diego, CA, facility and other Navy installations have conducted a six-month study on microprocessor and microcomputer standardization in Navy systems. As reported to Wescon by Ralph Martinez and Reeve Peterson, the study's key recommendations include:

★ Standardization on functional modules, which designers could interconnect to form computer systems.

★ Immediate interim standardization on one commercially available 8-bit CPU. The study concludes that technology has not yet advanced sufficiently to allow standardization on a 16-bit or bit-slice system.

★ Standardization on critical support modules. In decreasing priority, such modules include CPU support units; ROM/RAMs; UART/USRTs; PROMs; EPROMs; programmable parallel I/O interfaces, interval timers, interrupt controllers and DMA controllers; and multiply/divide units.

★ Selection of the CPU and support systems by competitive procurement.

Any one of several 8-bit CPUs could form the Navy's interim standard for µP systems.

★ Requirement of second sourcing for all modules, based on compatibility of pinouts, I/O buses, electrical systems, instruction sets and environmental specs.

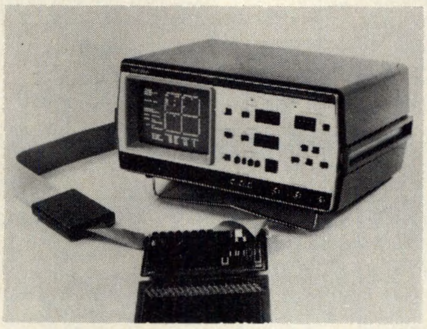
★ Provision of hardware support, including a prototyping system designed around the standard 8-bit CPU, and timesharing, batch and minicomputer systems that support the CPU's software.

★ Provision of software support, including a resident assembler and compiler on the prototyping system; editor, debug, diagnostic and utility programs; and cross-assemblers, a cross-compiler and a software simulator written in machine-independent ANSI Fortran IV.

Martinez and Peterson note that standardizing on a commercially available 8-bit microprocessor preserves assembly-language programming flexibility but "does not constrain the development and use of macro and higher-order languages." They recommend that specification of the 8-bit CPU and its support modules begin immediately, and that specification of a 16-bit CPU, its support modules, and the modules for a bit-slice system begin in six to nine months.

µP analyzer displays data in four formats, allows time- and data-domain studies

Utilizing separate personality modules to serve microprocessor systems based on the Intel 8080A and the Motorola 6800, a recently developed microprocessor analyzer captures firmware operations in real time and allows a designer to examine system activity displayed in four analysis formats. Acquiring data at up to 10 MHz, the analyzer can record the results of as many as 256 memory accesses.



Equipped with a personality module either for the Intel 8080A or the Motorola 6800, Biomation's Model 168-D microprocessor analyzer tracks a system's activity for up to 256 memory accesses and displays the results of those accesses in any one of four analysis formats.

Dave Blecki, VP for marketing at Biomation, explains that the Cupertino, CA, firm plans eventually to provide additional personality modules for the Model 168-D analyzer. He adds that the unit's 10-MHz recording rate suits it to analysis of both MOS and bipolar microprocessor systems.

Four display modes. The microprocessor analyzer captures 25 bits – 16 bits of address information, eight data bits and one bit that characterizes an operation as a read or a write – each time a microprocessor system under analysis performs a memory access. The unit can record the results of 256 such accesses for a given record sweep.

Once a sweep is complete, a designer can view the data, presented on a built-in 9" CRT, in any one of four display modes. Three of the modes show the data in hexadecimal form and the fourth provides a switch-selectable listing in hexadecimal or binary.

★ In its *memory display* mode, the Model 168-D displays a memory map organized into four 64-character groups; each character represents the most significant eight bits of an address word in one of the analyzer's 256 memory pages. An asterisk at a location in this array denotes one or more accesses to that location.

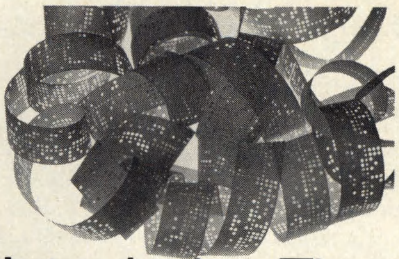
★ In its *page display* mode, the analyzer focuses on the contents of a single memory page, selected through a front-panel thumbwheel switch; it presents a map that shows the least significant eight bits of each address word on the page. By positioning a cursor on the number that denotes a specific memory address, a designer can observe the data resulting from the most recent access of that address. Decrementing the cursor shows earlier accesses.

★ In its *sequential display* mode, the analyzer presents a time-domain picture of system activity by displaying the results of a sequence of accesses in a 64 x 64 array; the most recent access occurs in the array's upper left-hand corner. Each access is identified as a read or a write.

★ In its *list display* mode, the 168-D shows the results of 20 sequential memory accesses at a time, arranged in order from top to bottom of the CRT. A designer can also choose to display this information in binary form to ease comparison of system activity with a source code or program listing.

System transparency. Designed to passively record data without affecting the performance of the system under development, the microprocessor analyzer can also halt at a preselected point. Then a designer can single-step the analyzer to pin down the steps that lead to an undefined or prohibited state.

Six front-panel BNC connectors allow external input of arm, start and stop signals, and a designer can choose positive or negative slope sensitivity for the start and stop signals.



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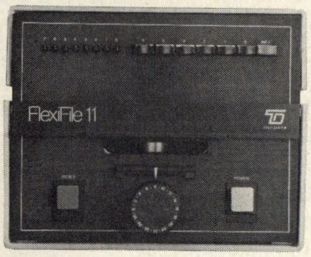

is user-defined. It's as easy as pushing the reset switch. 8 LED'S indicate each operating mode. 6 input switches let you determine the operating mode ... using your own protocols, control words, and commands. The FlexiFile 11 is Microprocessor Controlled and floppy disk based. Our fully modular interfaces include an RS 232 coupler, and IEEE-488 Instrumentation Bus, and an 8' Bit Parallel Bus.

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CIRCLE 21

Hardware and services

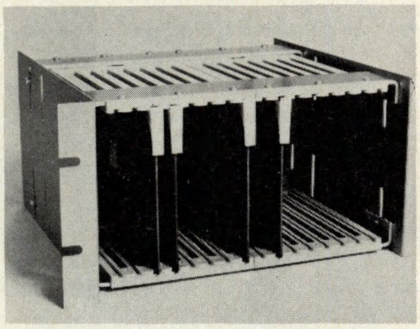
PROM programmer. Model 501 incorporates a set of hexadecimal displays to eliminate the need to translate addresses and data from binary. It also incorporates a hexadecimal keyboard. The programmer utilizes an 8-bit microprocessor and provides zero field test, automatically incremented address, straight PROM-to-PROM duplication, duplication with change in section of copy PROM, verification and step-by-step reading of PROM contents. Options include paper tape and Teletype interface; personality modules serve several types of MOS PROMs and fusible link PROMs. Price: $2150; personality modules cost approximately $500 depending on type. Technitrol, Inc., 1952 E. Allegheny Ave., Philadelphia, PA 19134. **Circle 126**

Z-80 microcomputer kit. The Quay 80AI microcomputer kit incorporates the Zilog Z-80 microprocessor and runs at 2.5 MHz. It requires a power supply and terminal device for independent operation, or you can plug its 100-pin edge connector into an Altair or Imsai bus in place of those units' 8080-based CPU boards. The kit also incorporates a ROM-based monitor that allows you to dump and load memory or change its location and to program UV-EPROMs. A serial I/O port permits use of RS 232C or 20 mA terminals at rates ranging to 2400 baud, and a parallel input port services an 8-bit ASCII keyboard and supports a memory-type tv monitor interface. Price: $450 in kit, $600 assembled. Quay Corp., P.O. Box 386, Freehold, NJ 07728. (201) 681-8700 **Circle 163**

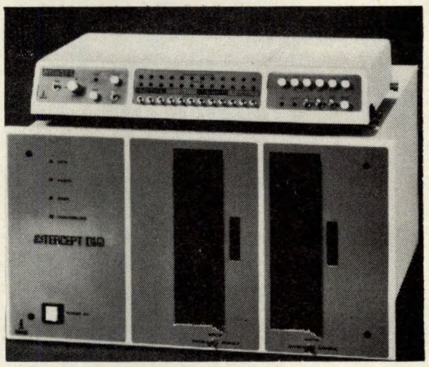
Cross assemblers for 6502, 6800 and 8080 μPs. Running on the DEC PDP-8 mini, the X8 series of cross assemblers each occupy 8K of memory and run under the OS/8 operating system. They utilize a universal assembler format of common assembler directives and techniques and provide pseudo-ops and run-time options for conditional assembly and listing control. The assemblers support arithmetic and logical operators in complete operand expression evaluation and output generated object code in a microprocessor's standard loader format or in BNPF format for ROM generation. Price: $400 each on paper tape, Dectape or DEC floppy diskette. Cross assemblers for the 2650 and F8 microprocessors will appear soon. Sierra Digital Systems, 1440 Westfield Ave., Reno, NV 89509. (702) 329-9548 **Circle 127**

Short course with take-home μC. Scheduled for presentation in Boston; Chicago; Dayton, OH; Huntsville, AL; Los Angeles; St. Petersburg, FL; Palo Alto, CA; Philadelphia; and Washington, DC, this 3-day course will cover microprocessor hardware, software, firmware and economics. Attendees at the February and March sessions will receive the organizer's Wince 6800-based microcomputer to use during the course and to take home. Fee: $495. Wintek Corp., 902 N. 9th St., Lafayette, IN 47904. (317) 742-6802

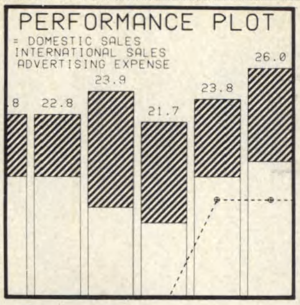
8080A card racks. Designated CRS-81 and CRS-82, these expandable 8080A microprocessor card rack systems come prewired for 10 cards with connectors for 16 cards. The 4-card CRS-81 system uses 1702A PROMs and includes an 8080A microprocessor, 1K words of RAM, sockets for 2K words of ROM, four 8-bit input ports, four 8-bit output ports, DMA and interrupt, and a 1-μs state time crystal clock. You can expand the system to 6K of ROM, 5K of RAM, eight 8-bit input ports and eight 8-bit output ports. The 3-card CRS-82 system uses 2708 PROMs and includes an 8080A microprocessor, 1K words of RAM, sockets for 4K words of ROM, four 8-bit input ports, four 8-bit output ports, DMA and interrupt, and a 0.488-μs state time crystal clock. You can expand this system to 12K of ROM, 13K of RAM, eight 8-bit input ports and eight 8-bit output ports. Prices: $550 for the CRS-81, $505 for the CRS-82, both in 25-99 quantities. Pro-Log Corp., 2411 Garden Rd., Monterey, CA 93940. (408) 372-4593 **Circle 131**

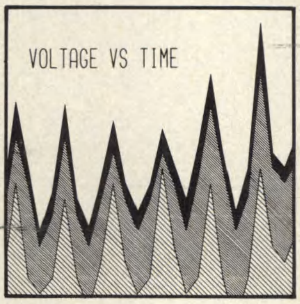


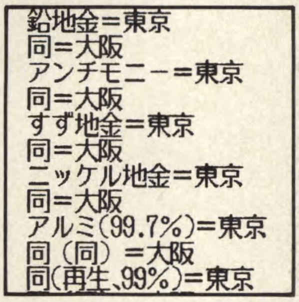
Floppy-disk development system. For use with the manufacturer's IM6100 Intercept prototyping system, the 6970-IFDOS consists of two interfaced floppy-disk drives plus electronics, power supplies and cables. All components come in one covered enclosure, which you can rack- or tabletop mount and which plugs into Intercept. The device is fully software compatible with the Digital Equipment Corp. RX8 flexible disk system for the PDP-8/E minicomputer. Software components include a file system, a keyboard monitor, a text editor, an assembler, a binary loader, an octal debugger, a high-level language interpreter, and utility programs. Price: $5100. Intersil, 10900 N. Tantau Ave., Cupertino, CA 95014. (408) 996-5000 **Circle 130**



Intellec and MDS operating system. Designated SLAM, this operating system serves Intel's Intellec 8/Mod 80 and MDS microcomputer systems. It provides a text editor and high-level language interpreter and occupies less than 3200 memory bytes. You can create a program using the text editor then run it immediately using the microcomputer and a teletypewriter, thereby eliminating paper-tape operations without adding a diskette. The language resembles Basic and is loaded and entered with Intel's System Monitor. It comes on paper tape, ready to load without modification. Price: $99. Specify whether you require interrupt capability. PennMicro, P.O. Box 5073, Lancaster, PA 17604. (717) 569-8032 **Circle 161**



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同＝大阪
アンチモニー＝東京
同＝大阪
すず地金＝東京
同＝大阪
ニッケル地金＝東京
同＝大阪
アルミ(99.7%)＝東京
同（同）＝大阪
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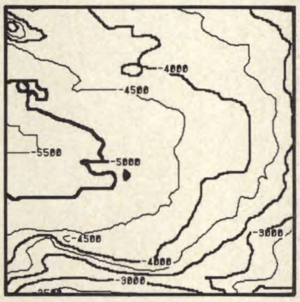
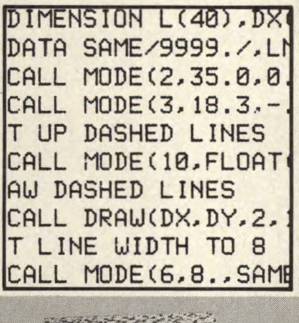
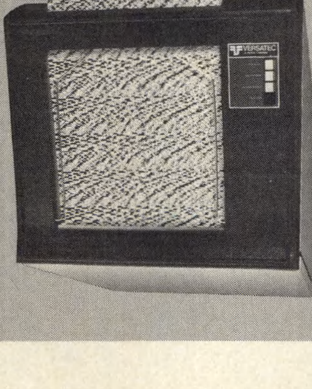




```
DIMENSION L(40),DX
DATA SAME/9999./,L
CALL MODE(2,35.0,0
CALL MODE(3,18.3,-
T UP DASHED LINES
CALL MODE(10,FLOAT
AW DASHED LINES
CALL DRAW(DX,DY,2,
T LINE WIDTH TO 8
CALL MODE(6,8.,SAM
```



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computer model and operating system

application

name telephone

organization

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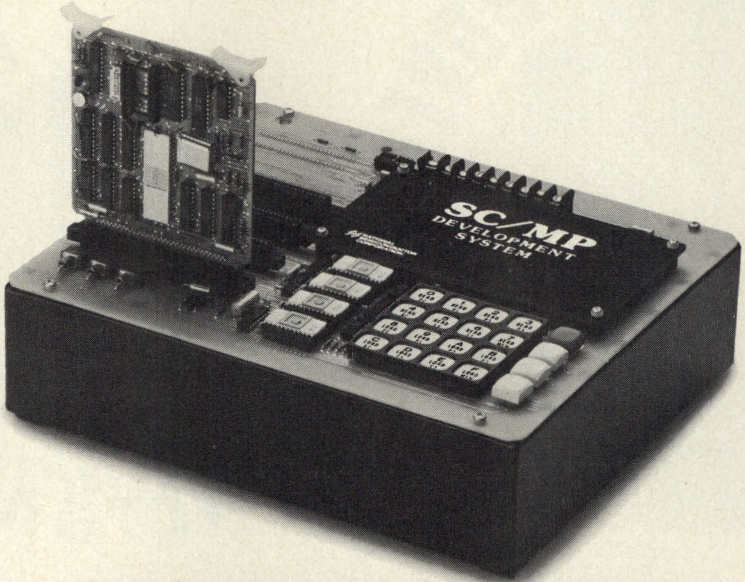
city, state & zip

CIRCLE 22

SCRIMP W

ITH SC/MP.



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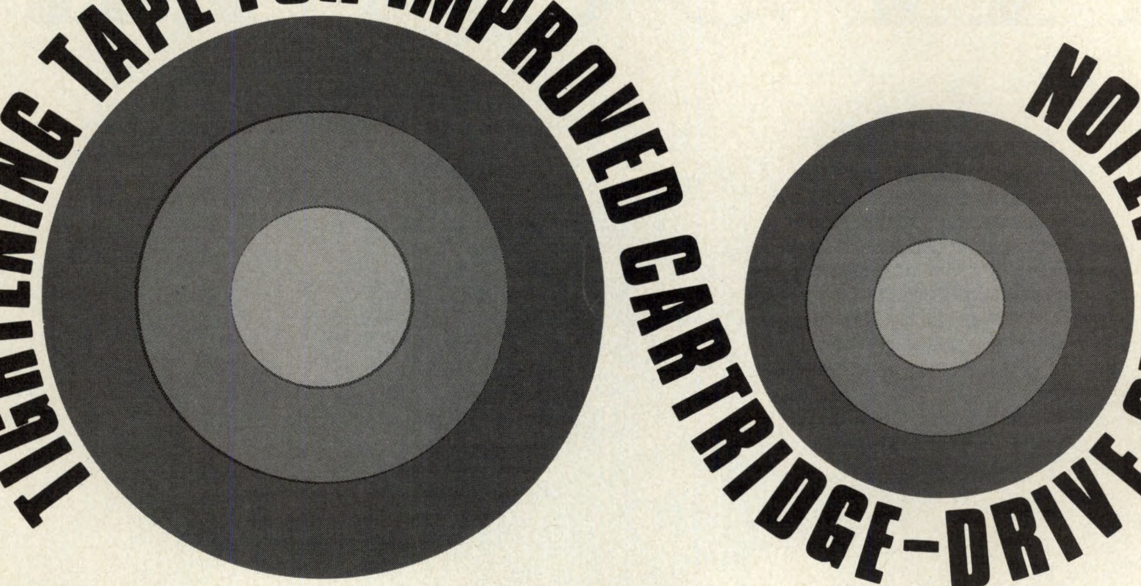


by **Bansi Shroff**

DUAL-SPRING REEL-BRAKE SYSTEM GIVES ½" TAPE CARTRIDGE DRIVE A REEL-TO-REEL DECK'S PERFORMANCE

Our primary design goals in developing a cartridge tape drive that incorporates most of the features of a ½", IBM-compatible digital reel-to-reel tape deck centered on four basic considerations:

★ A cartridge provides media protection from the environment, as well as from operators' fingers.
★ A cartridge drive is comparable in size to a floppy-disk drive but records at up to 50 times the bit density.
★ A cartridge drive can be impervious to large changes in temperature and humidity.
★ A cartridge is inherently much easier to load and unload than tape reels on a standard deck.

The result of our efforts, the 2000 Series Tape Pac system (Fig 1) uses ½" computer-grade tape in its cartridge and read/writes at up to 60 ips. The system's rewind and fast forward speeds equal 240 ips, and its cartridge – which holds 1000 ft of 0.5-mil tape – can store 153 Mbytes of data recorded at 1600 bpi (standard 9-track phase encoded format). Other available cartridges house 450 ft of 1.5-mil tape (69-Mbyte capacity) and 600 ft of 1.0-mil tape (92-Mbyte capacity).

We achieve the required resistance to temperature and humidity changes with a dual-capstan drive system, in which a pair of elastomer-coated capstans contact the peripheries of the takeup and supply rolls within the Tape Pac cartridge. The pressure applied by these capstans to the tape rolls keeps the tape very tight on the rolls. Tightly packed tape rolls have little air between their adjacent layers; the tape is thus less susceptible to expansion or contraction due to temperature or humidity variation. We easily meet an operating temperature spec of 0 to 55 C and a humidity spec of 5 to 95%.

Bansi Shroff *is a senior engineer at Emerson Electric's Industrial Controls Div., Santa Ana, CA.*

design methods ensure interchangeability

Because reliability and interchangeability of cartridges between drives are mandatory in this type of system, we took special care to follow high-precision design procedures. Each cartridge stores tape in a reel-to-reel configuration on flangeless reels mounted in a high-impact, die-cast aluminum container that incorporates tape guides. Spring-loaded dust doors close and self-energizing reel brakes within the cartridge automatically lock the reels when a user removes the cartridge from the transport. A file protect switch also safeguards data recorded on the cartridge.

When the user inserts the cartridge into the drive and closes the transport door, the capstans engage the tape reels on their peripheries. Independently driven by separate motors and controlled by a servo system so that the takeup unit runs slightly faster than the supply unit, the capstans provide constant tape tension across the drive's heads. As the tape moves and the diameters of the tape on the takeup and supply reels change, the capstans slide back and forth under controlled tension.

design problems materialize

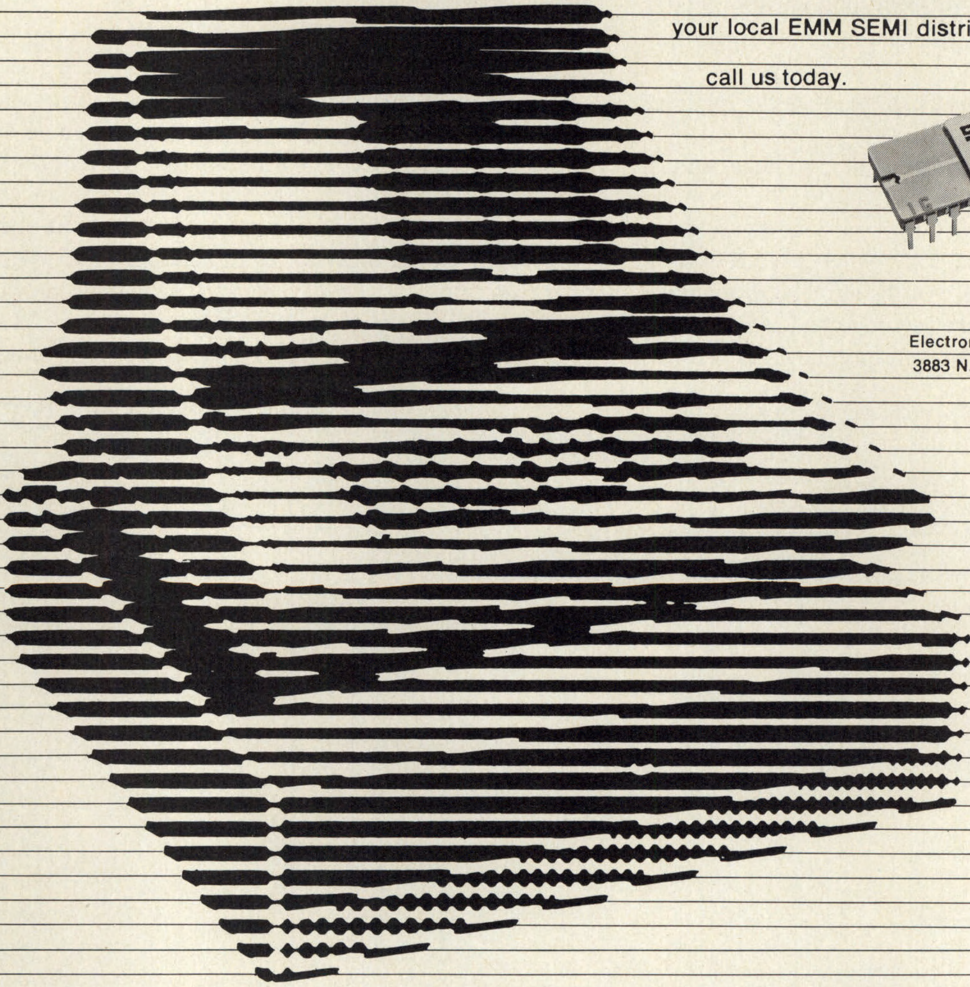
Designing the unit involved solving the usual quota of difficult problems. Our most serious problems were in five areas:

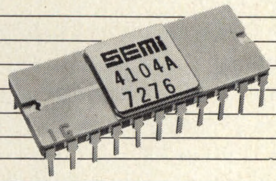
★ Inserting the cartridge into the drive without misalignment

MEMORY AT WORK

Retail Sales

The point of sale terminal is just one application where data integrity and ease of maintenance are vital. The SEMI 4104A static 4K RAM answers both problems perfectly. It is static; that means simpler, faster field maintenance. And just 15 mw will protect data. The 1K x 4 organization is ideal for small capacity systems, and the 200 nsec access (350 nsec cycle) time makes it fast enough for any 8080A class microprocessor on the market. Get full details from your local EMM SEMI distributor, or call us today.





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CIRCLE 23

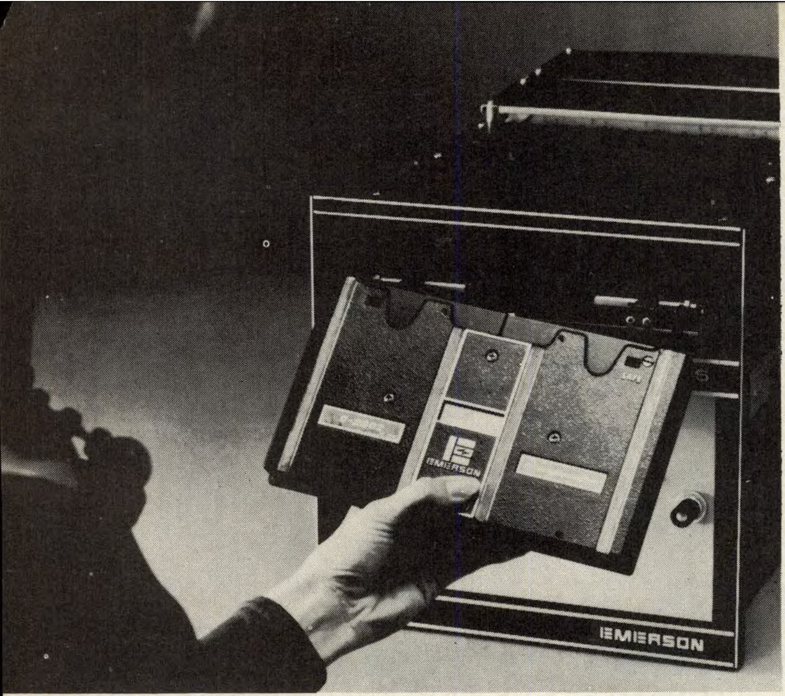


Fig 1 Tape Pac stores 153 Mbytes recorded at 1600 bpi on 1000 ft of 0.5-mil ½" tape. Elastomer-coated capstans in the drive contact the peripheries of the takeup and supply reels in the cartridge; the pressure on the reels keeps the tape tightly packed and relatively insensitive to temperature and humidity variations.

★ Guiding the tape in the cartridge without tension variation

★ Protecting the medium from wandering fingers when the cartridge is out of the drive

★ Keeping the tape tight in the cartridge when the cartridge is out of the drive

★ Designing a relatively cheap servo system to maintain tape speed to within 2% and control tape tension.

To achieve "foolproof" cartridge insertion, we designed guide rails in the door to mate with reference lands in the cartridge as the cartridge slips past the door. Additionally, the sides of the door center the cartridge, and as the cartridge passes the door, pressure pads push down on its sides.

Before a user closes the door, the cartridge is locked in place by lever detents; the user must close the door before the drive will operate. To remove the cartridge, the user must first press a release bar to disengage the lever detents; the spring-loaded capstans then push the cartridge toward the door. Grabbing a finger hold on the end of the cartridge then lets the user remove the cartridge from the drive.

Our original design didn't incorporate a release bar and lever detents to hold the cartridge in place; the door pushed the cartridge into place and seated it when closed. And the lack of rails on the door sometimes allowed the cartridge to misalign and thereby jam the system.

To provide accurate tape guiding, we first considered using fixed guides fabricated from either metal, plastic or glass. But the wrap angle of the tape on fixed guides was too great, and the resulting tension would have varied by almost 100%. So we chose instead to use rotating guides of Rulon, a material manufactured by Dixon Corp., Bristol, RI. These guides allow a bidirectional tension variation of less than 10%.

We could have provided media protection in several ways for cartridges removed from the drive; we focused on building spring-closure doors onto the cartridge. Automatically opened by the transport when the cartridge is inserted into the drive, the doors act like levers pivoted on a fulcrum and are operated by pressure plates on the side walls of the cartridge-insertion opening.

reel brakes tighten tape

Many cartridges experience accidental tape spillage when removed from their drives. To prevent this problem in our drive we devised a reel-brake system that tightens the tape on the reels whenever the cartridge is removed from the drive. We could have used a band around the hubs tied to a fixed point with a single spring to maintain band tension, but that approach doesn't increase the tape tension when the cartridge is out of the drive.

A better solution, we feel, utilizes a two-spring mechan-

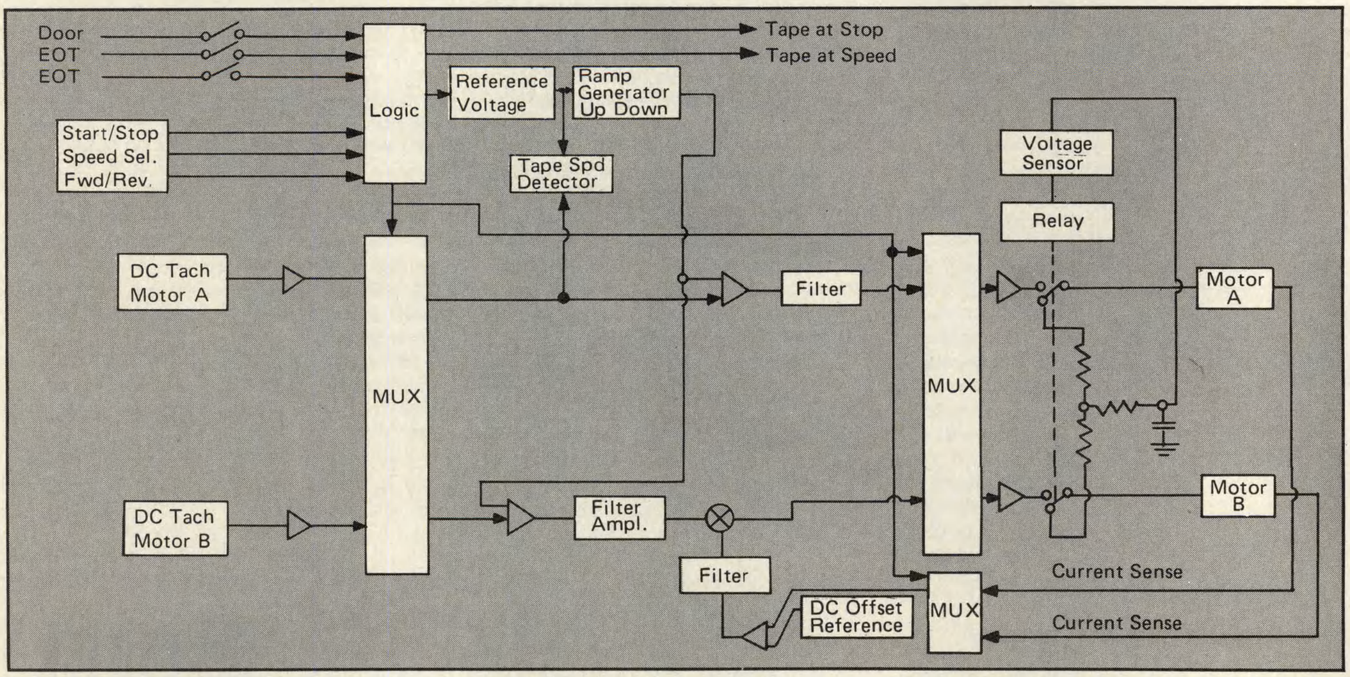
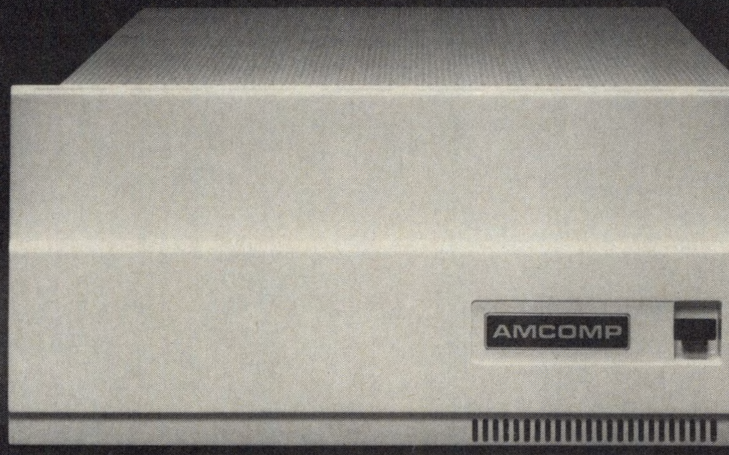


Fig 2 Velocity servo incorporates a reference-voltage adjustment to facilitate speed selection. Supply-reel speed is slower than takeup-reel speed to ensure proper tape tension; if power fails, the system switches the drive motors in series to brake each other.

Our statement on high density head-per-track disc technology:

“



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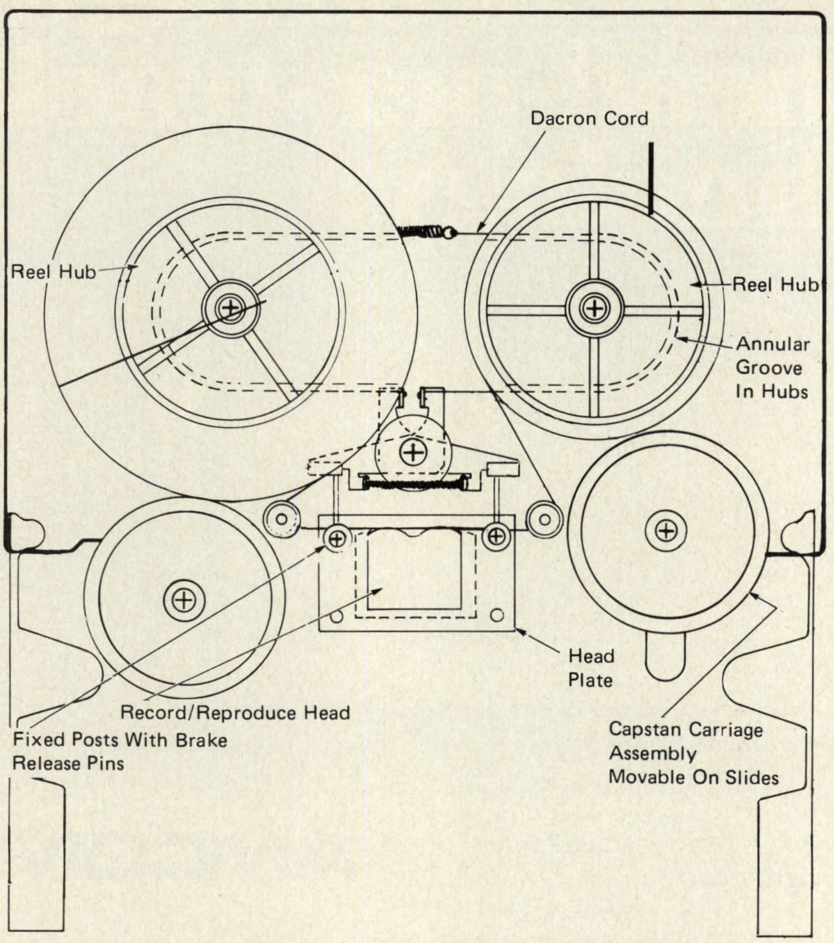

Fig 3 Two Dacron cords in the tape cartridge wind around the cartridge's hubs and connect to two helical springs and a wing pivot. When the cartridge is placed in the drive, two pins push against the wings and release the tension on the cords.

ism (Fig 3). Each of the reel hubs contains an annular groove below the surface on which the tape is wound; separate Dacron cords wrap around the annular groove in each hub. One end of the cord from each hub attaches to a light helical spring at the rear of the cartridge, and the other end of the cord from each hub connects to an arm of the brake actuator. These two arms pivot on a shaft mounted on the upper and lower walls of the cartridge casing, and a second, heavier helical spring connects the wings of the two arms.

With the cartridge in the transport, brake release pins on the fixed posts of the head assembly insert through holes in the cartridge, push against the two wings of the brake actuator and spread the two arms apart to release the tension on the Dacron cords and spring. This action allows the capstan drive to control the reel motion within the cartridge.

When the cartridge is removed from the transport, the brake release pins allow the spring to pull the arms of the brake actuator together and thereby draw the Dacron cords tight. The two hubs then rotate in opposite directions and draw the tape in the cartridge tight. In this position, the Dacron cords form an effective brake around the hubs; if the cartridge is shaken or vibrated, the brake system actually tightens the tape.

velocity servo accurate to 2%

To maintain tape speed past the heads constant to within 2%, control tape tension and keep costs low, we examined several designs for a velocity servo controller. Our first designs were phase-lock approaches; one dual phase-lock system worked well but was too complex and expensive. A second approach combined a single phase-lock with a velocity servo; it required impractical changes in amplifier gain and reference voltages.

In our final design (Fig 2) a pair of dc motors drives the capstans, and dc tachometers monitor motor speed. The speed selector on the drive sends a signal to motor-control logic, which selects a voltage reference that the motor speed is set against.

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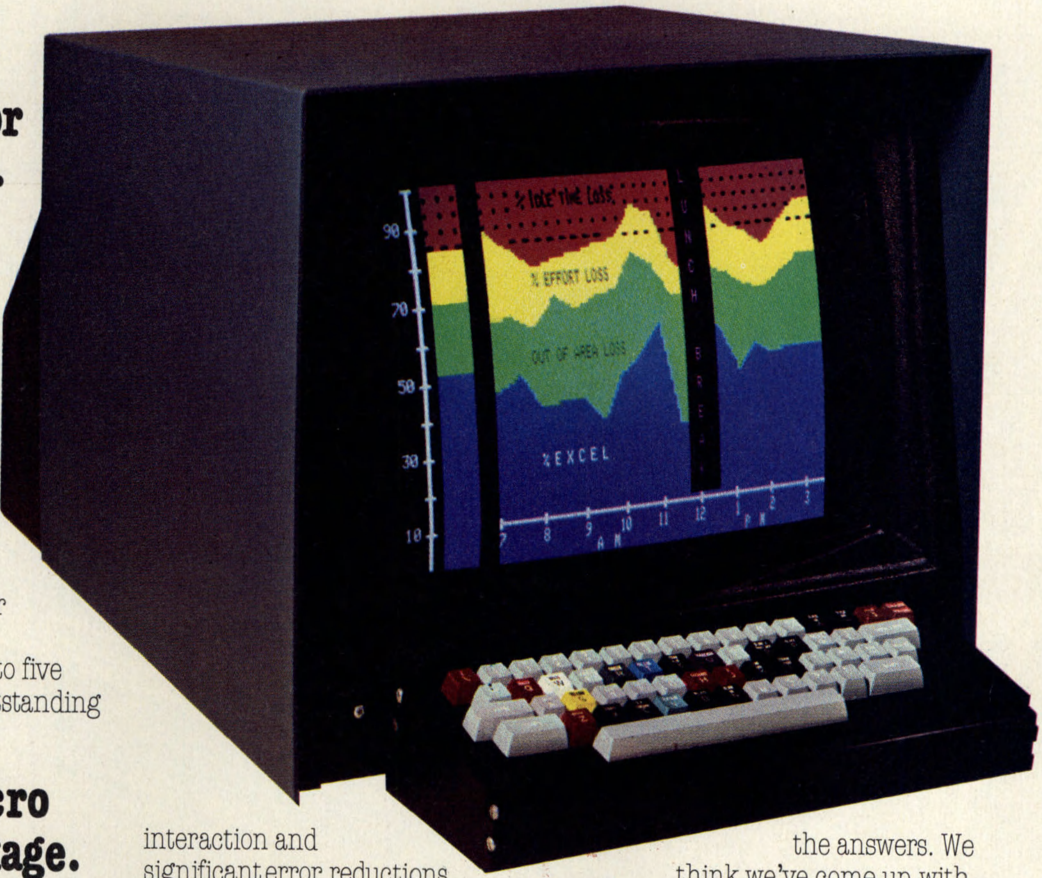

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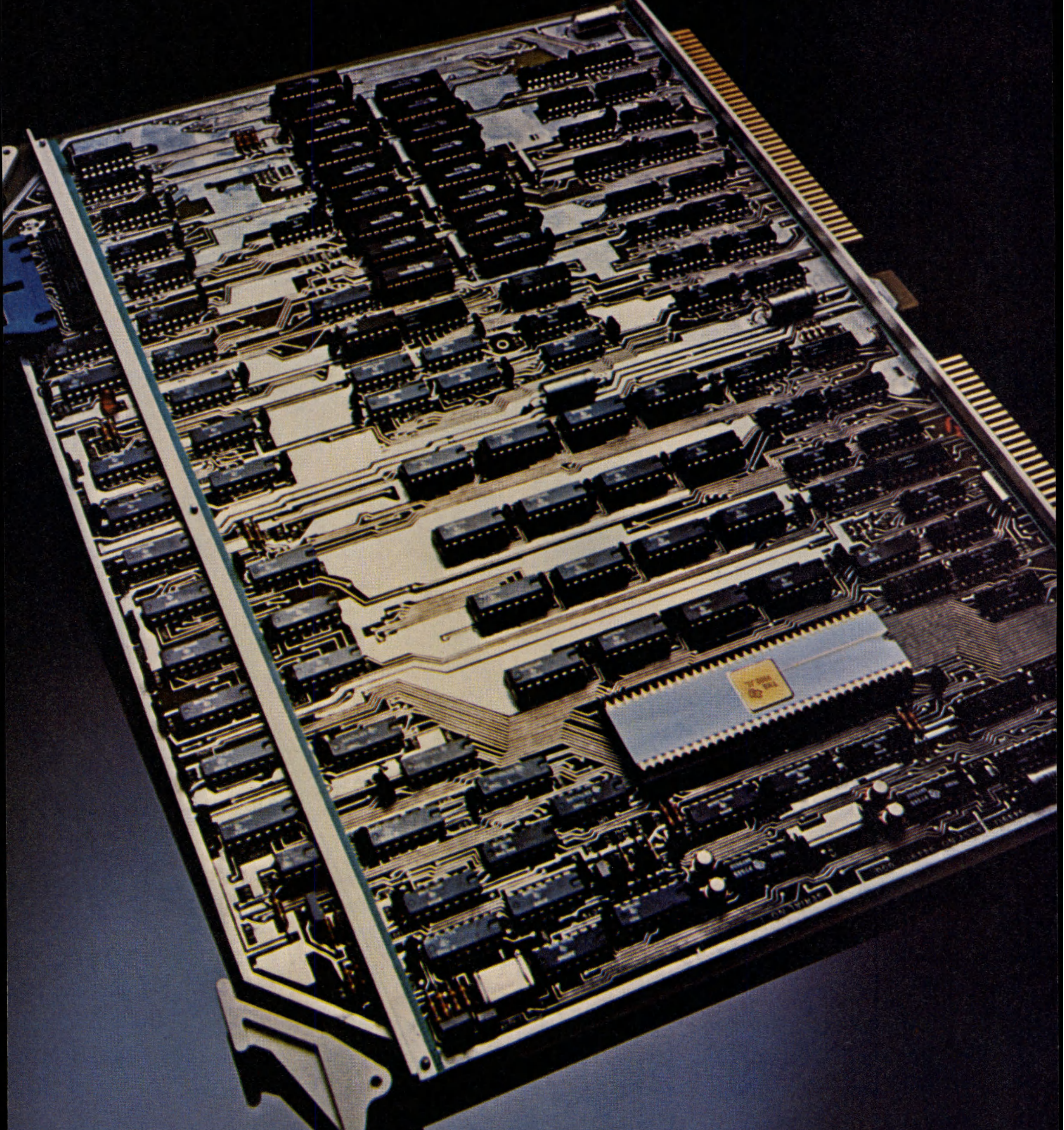

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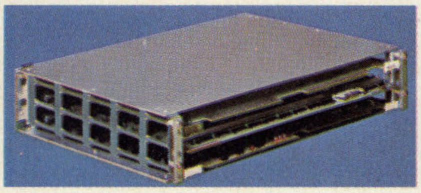

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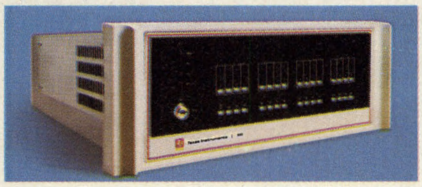

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EDUCATING 'DUMB' DATA ACQUISITION SUBSYSTEMS

by **Lewis Solomon** and **Edward Ross**

Part Two: How do data acquisition subsystems communicate, and what design decisions face their manufacturers in the quest for greater subsystem intelligence?

Last month we reviewed subsystem architecture, surveyed the structure and operation of some subsystem components and discussed the characteristics of three important classes of subsystems: modular/PC board units; "standard" (rack-mounted), non-intelligent units; and intelligent subsystems. We also discussed some of the factors that we believe govern current and future microprocessor usage in intelligent subsystems. We begin this concluding installment by focusing on a fourth important group of data acquisition subsystems – communications oriented units.

Effective communication between two data acquisition devices, like communication between two humans, requires two essential elements: an effective speaker and a skilled listener. Because data acquisition systems contain many devices, they require many communication links or interfaces. Engineers have expended much time, energy and expense in developing interfaces that have proven less than optimum. A data acquisition subsystem generally is a collection of different kinds of hardware – frequently utilizing unrelated technologies – which must function as a unified whole. Currently, interfacing these diverse pieces of equipment is difficult because of a complete lack of standardization.

A single communication-system philosophy appears unlikely to solve everyone's interface problems. In implementing communications oriented data acquisition subsystems, manufacturers must select a limited set of objectives that will suit a broad range of functions including measuring, displaying, computing, storing and interfacing a variety of devices. Such subsystems cannot be based only on large computer controlled installations; they must also be compatible with low-cost systems. Unless the cost of the communications hardware and software is low in relation to the cost of the data acquisition hardware, most available techniques become difficult to justify.

Much equipment for solely digital systems is advertised as "plug-to-plug compatible." Achieving this goal in data acquisition subsystems implies much more than mere agreement on the hardware aspects of a communications interface. A comprehensive solution requires the industry-wide adoption of an interface philosophy to provide flexible communications between devices at reasonable cost. Manufacturers and users must agree on message content, on techniques for exchanging data, on codes, formats, logic conventions, timing, control techniques and software.

The problem of communications in data acquisition subsystems is complex and cannot be resolved solely on the subsystem level; the component and system levels are important too. For example, at the component level, manufacturers will have to decide to standardize on address selectable A/D converters that have TTL-compatible (or CMOS-compatible) tri-state outputs and can provide digital data in both serial and parallel form. At the subsystem level, manufacturers will have to agree on multiplexing schemes, bus structures and encoding techniques. At the system level, agreement must appear on system partitioning, digital vs. analog signal transmission, dedicated on-line shared approaches, cabling cost considerations, data acquisition vs. control techniques and software vs. hardware considerations.

We focus here on data acquisition subsystems based either on a communication scheme internal to the equipment or on a communication scheme that facilitates external communications between data acquisition subsystems and computer oriented devices.

communication techniques and computer interfaces

In laboratories, factories and process plants, electronic equipment finds increasing usage, and the data generated by this equipment has put heavy demands on available communications facilities. The result? Users have experienced serious

Lewis Solomon *and* **Edward Ross** *are respectively president and senior consultant at Venture Development Corp., a Wellesley, MA, management consulting firm that serves the electronics industry.*

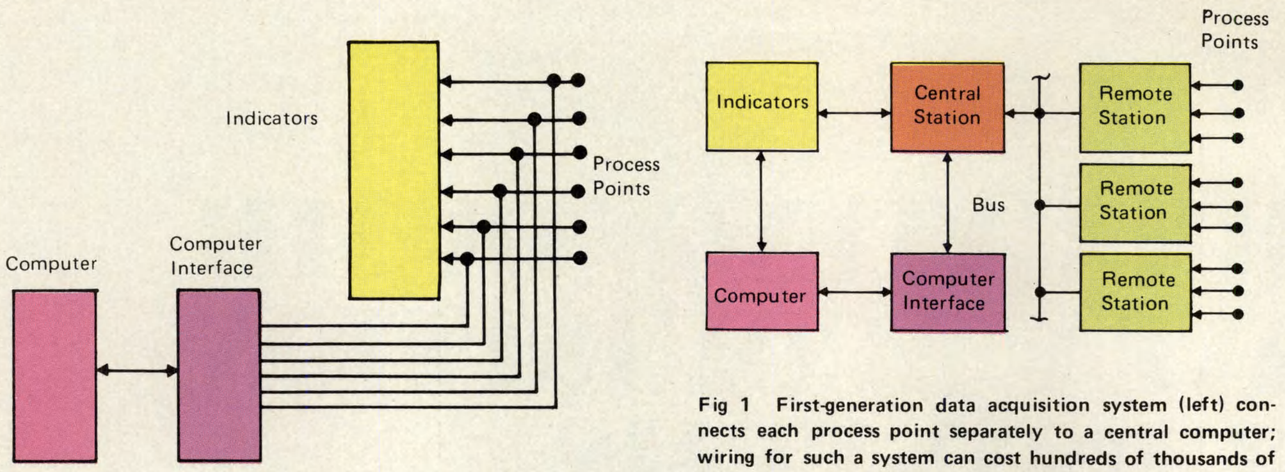

Fig 1 First-generation data acquisition system (left) connects each process point separately to a central computer; wiring for such a system can cost hundreds of thousands of dollars. A second-generation system (right) utilizes modular equipment and line-sharing techniques to alleviate this cost problem.

problems with cable congestion, wiring costs and lack of flexibility in existing systems. First-generation data acquisition systems were highly centralized; each monitored point was separately wired to the computer in the control room. Some systems monitor more than 1000 points, and many of these points are 1000 ft from the control room. In such systems, wiring costs hundreds of thousands of dollars and modifications are difficult.

Current second-generation subsystems alleviate these problems by utilizing building-block and line-sharing techniques. The building-block or modular technique allows a user to select from several self-contained functional elements designed to work together. The modules incorporated into second-generation subsystems provide data only on receipt of appropriate addresses. Manufacturers of second-generation subsystems attempt to solve wiring problems by using line-sharing approaches that allow a few wires to carry the data and control signals that formerly were handled by a multitude of wires; line-sharing systems utilize time division multiplexing and party line configurations. Fig 1 contrasts a first-generation system with a second-generation one. The RTP subsystem from Computer Products, Inc., is an example of a pioneering, and well accepted, second-generation subsystem.

In line-shared subsystems, signals originating at and returning to individually monitored points go sequentially along one time-division communications channel; such subsystems use party line or multiplexing techniques or combinations of both. In a party line arrangement, several monitored points in different locations connect in parallel across a single channel, typically a twisted pair. In a multiplexing arrangement, several monitored points connect to a single remote unit. One common configuration combines party line and multiplexing arrangements, and other configurations are also possible (Fig 2). A party line need not use one continuous conductor but can branch throughout a plant to minimize wire runs; branching improves reliability because it reduces the number of points dependent on one section of cable.

A further refinement is the common bus structure architecture, which in addition to providing flexibility and reducing wiring costs, increases data transfer capability. The architecture assigns to all or part of the system a priority over the computer, and the bus is a single party line path that connects all portions of the system in parallel. Not only can the CPU communicate with memory and I/O equipment, but any functional element can communicate with any other element. Several devices can often try to gain access simultaneously, so hierarchies of priorities are usually established.

Manufacturers of data acquisition subsystems must facilitate the interfacing of their equipment to computers. They can provide computer interfaces and thereby gain a competitive advantage, or they can choose not to provide interfaces and thereby eliminate involvement in numerous problem areas. Many manufacturers provide only multiplexed A/D converters; others give the user choices with regard to BCD, binary or tri-state outputs to simplify the user's interface design. Other manufacturers have developed circuits that interface their products to DEC, Data General, Hewlett-Packard and Intel minicomputers and microprocessors; some even provide applications assistance to customers with less popular minicomputers and microprocessors. By letting the computer manufacturers, the systems houses and the end users deal with the interface problem, data acquisition subsystem manufacturers risk lower levels of business.

Three types of computer interfaces exist: legislated industry standards, *de facto* industry standards and no standards at all. Except for the Teletype port's current loop interface and the Electronic Industries Association's RS 232C interface, no standard computer interface exists for subsystem makers to base a design upon. From a practical point of view, Camac and the H-P interface bus, while agreed upon, are too new and not well accepted enough to currently form industry standards.

Systems utilize either asynchronous or synchronous data transmission techniques. For synchronous systems, character location is indicated by a special synchronization pattern presented at the start of data transmission. Subsequent bit locations are determined by a transmitter and receiver that individually track a common clock. A new data bit is transmitted

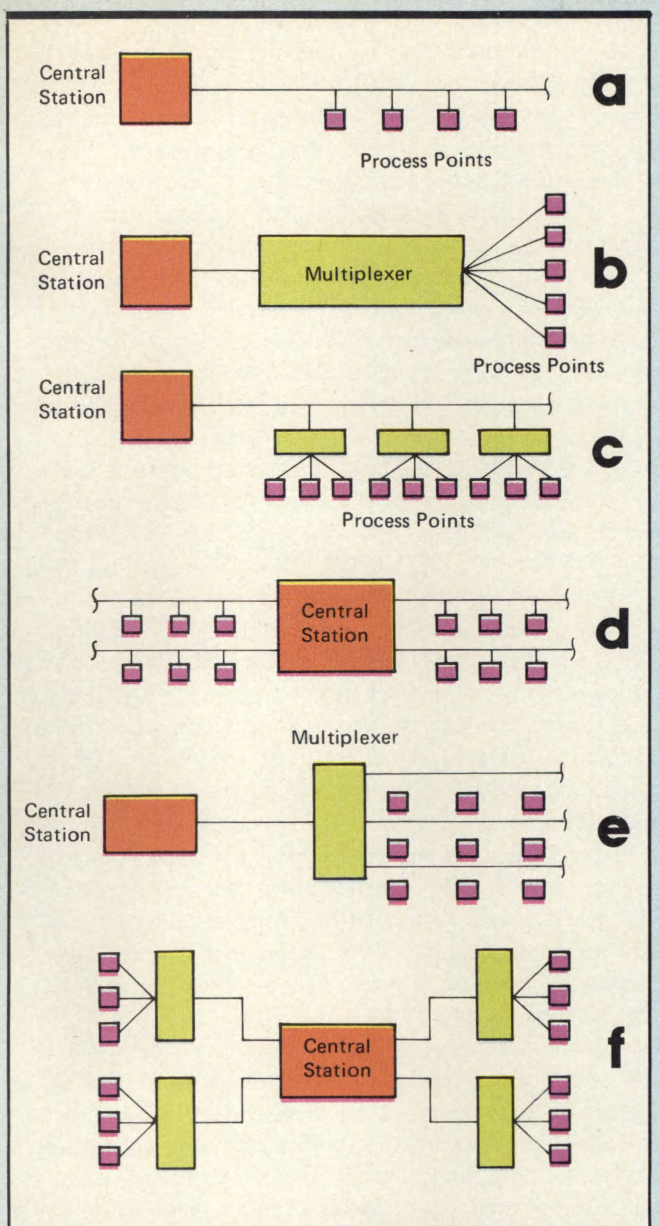

Fig 2 Line-shared subsystems utilize party-line techniques (a), multiplexing arrangements (b) or a combination of party-line and multiplexed communications (c). They can also incorporate multiple party lines hooked to a central station (d), multiple party lines connected to a multiplexer (e) or multiple multiplexers hooked to a central station (f).

every clock period after the sync pattern, and the clock must connect to both the transmitter and the receiver. In asynchronous systems a clock is not transmitted; instead, start and stop elements are added to each character to tell the receiver when to accept it. The start element is a space one bit long; the stop element is a mark one or two bits long. The negative-going transition of the start bit defines the beginning of a character and resets a counter in the receiver, and the receiver clock cycles are then counted to locate the center of the start bit and each subsequent bit.

The 20 mA current loop is a serial interface that turns current on and off and senses the presence or absence of current. RS 232C is an electrical standard for serial binary-data interfaces; it sets standards for voltages, impedances and currents. An RS 232C system can interface with most slow-speed devices that communicate in serial code; every CRT, teletypewriter, modem and computer comes with this interface. Sometimes a data acquisition subsystems manufacturer can simply specify RS 232C and thereby solve all interface problems. But problems can arise when RS 232C interfaces one piece of computer oriented equipment with another piece of computer oriented equipment, rather than data communications equipment. Connecting data acquisition subsystems or CRTs to minis is not as easy as it might appear; the process requires special adapters with unique wiring. It is not unusual to have problems with the request-to-send, clear-to-send, data-set-ready, data-terminal-ready, received data and transmitted data signals. And RS 232C does not define the coding to be transmitted across the interface; the most commonly used code is 7-level ASCII, but any other appropriate code is also permissible.

The ASCII format finds uses in communications between remote data acquisition subsystems and central computers located far from the measurement point. ASCII coded address symbols can be used to poll measurement points, select desired channels, specify measurement parameters and perform other command/control functions. Standard telephone lines handle ASCII for distances up to two miles, and a modem at each end of such lines removes all limits to transmission distance. ASCII is also ideal for those few applications requiring rf links, although modems are also needed to convert to FSK for modulation purposes.

During the past few years, IBM has gradually announced a new communications "standard" – SDLC (synchronous data link control) – and has indicated that it will be the only serial-by-bit synchronous transmission method the firm will support. Data acquisition subsystem manufacturers, as well as others who intend to communicate with IBM equipment, may have to adjust their designs to this *de facto* standard.

As a link control, SDLC deals with communication procedures between remote and controlling stations and provides only for station addressing, not for device addressing, source identification or destination addressing. It can convey the information for device identification and network switching, but its prime function is to serve as a means for a central station to control logical links to one or more remote stations on a line. All SDLC commands, polls, data and acknowledgements are sent in an array of "fields" termed a frame. SDLC does not specify the length of the information field, its internal grouping into bytes or the meanings of the bytes or byte sequences, and additional fields must maintain defined length and content. When timed data is not available, an NRZI coding accommodates asynchronous transmission.

Faster data exchange between a computer and a data acquisition subsystem requires using the computer's I/O system, for which no standards at all exist.

Three methods exist for transferring data into or out of a computer: programmed I/O, direct memory access (DMA) and interrupt data transfer. In *programmed I/O,* the computer controls data transfer independently of the data acquisition peripheral, and transfer occurs on a single-word basis. This interface finds few uses because the computer gets tied up waiting for slow devices. *DMA interfaces* allow block transfer of data into or out of memory at high speed, limited only by memory cycle time, and are commonly used for data transfer to and from mass storage devices.

Cont'd p. 40

During *interrupt data transfer,* the peripheral interrupts the program when it is ready to transfer or receive data. Low- and medium-speed devices – like data acquisition subsystems – use this type of interface.

Data acquisition subsystem manufacturers have attempted to solve interfacing problems by designing interfaces that serve specific popular minicomputers; by designing computer-independent interfaces (i.e. Teletype interfaces); by hoping for industry standards to become widely accepted; or by ignoring the problem. The advent of the microprocessor has served to further complicate the interfacing problem. We feel that microprocessor manufacturers should standardize on the I/O interface signals and handshake protocols of the popular minicomputers so as to make minicomputer and microcomputer interfaces indistinguishable from the data acquisition subsystem user's viewpoint.

While microprocessors can complicate some aspects of the interfacing problem, other LSI circuits make life easier. We believe Signetics and SMC Microsystems are developing SDLC I/O LSI chips for users who wish to adopt the IBM protocol. Several companies sell UARTs (universal asynchronous receiver transmitters), PSARs and PSATs (programmable synchronous/asynchronous receivers and transmitters), and ACIAs (asynchronous communication adapters). These LSI circuits are used by data acquisition subsystems manufacturers in asynchronous data communications applications at transmission rates below 1200 bps or 120 char./sec.

Camac. A line-sharing system first proposed in March 1964, Camac (Fig 3) was first developed by the ESONE Committee of European Laboratories and was endorsed in March 1970 by the U.S. Atomic Energy Commission's NIM Committee as a dataway system complementary to the NIM (nuclear instrument module) system. It is an internationally accepted standard that specifies the electrical, mechanical and functional characteristics of devices that handle data exchange with each other, with computers and with computer peripherals. More than 60 companies in ten countries have developed Camac-compatible product lines. Because Camac is a non-proprietary specification that can be adopted and used free of charge by any organization without any form of legal agreement, many Camac-compatible products have been developed with the same module sizes, card cages, specifications, ground planes, connector pinouts and data communications capability. In addition, Camac equipment can be used with most computers. Copies of the Camac standard are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402. Ask for documents TID-25875, TID-25876, TID-25877, TID-25878 and TID-26488.

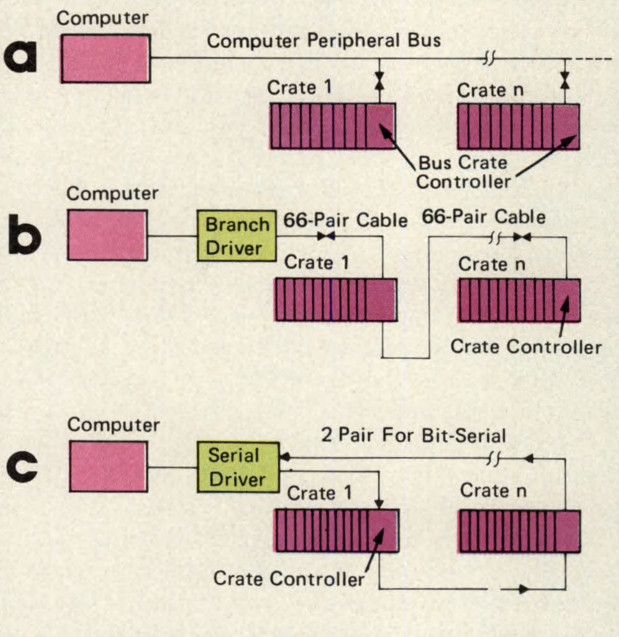

Fig 3 Camac line-sharing system utilizes standardized functional modules that connect to a computer's I/O bus(a). A 66-circuit bus termed a branch highway (b) provides parallel interface capability, and a 2-circuit bus termed a serial highway provides serial interface capability (c).

Camac is a parallel bus consisting of 86 lines running in daisy-chain fashion between devices and to a computer. Termed a dataway, the parallel bus provides the path along which digital data, control signals and timing signals travel. Each Camac module contains control circuits that can decode an initiated function, recognize a requested address, generate interrupts and detect errors. In addition, each module contains the circuits for its specific function, for example, A/D, D/A and multiplexer. Common "initialize," "clear," and "inhibit" circuits allow system startup and control. The data path is 24 bits wide; modules can use any word length up to 24 bits and are addressed by their position in the rack or crate. Each position has an individual interrupt line.

Communication along the dataway is managed by a crate controller mounted in the two right-hand slots of the crate. The crate controller provides the buffering and control functions required to interface the dataway with the Camac data bus, and it speaks directly to the modules, which speak back to it. Modules cannot speak to each other or to the outside world without the controller acting as an intermediary, however.

In a small self-contained system such as a data display subsystem, the modules speak to the controller, and the controller speaks only to the modules. In a slightly more complex system like a data logger, the controller can act as a go-between for modules and the peripheral driver required to drive a magnetic tape unit. Where computers are involved, a branch driver conducts two-way conversations with the controller and the computer.

Two Camac data buses exist: a 66-circuit parallel bus called a branch highway and a two-circuit serial bus called a serial highway. Branch and serial drivers interface these highways to a computer; drivers exist for most popular computers. Crate controllers can also interface the dataway directly to a computer's I/O port. Data transfer occurs bidirectionally, and the timing of the branch highway involves "handshake"-type operations to make the system's functions independent of signal transit times.

Large and medium-sized Camac systems are generally programmed in Fortran with standard calls for the modules used. The module routines then call a Camac routine unique to the particular computer and Camac interface;

CIRCLE 27 ▶

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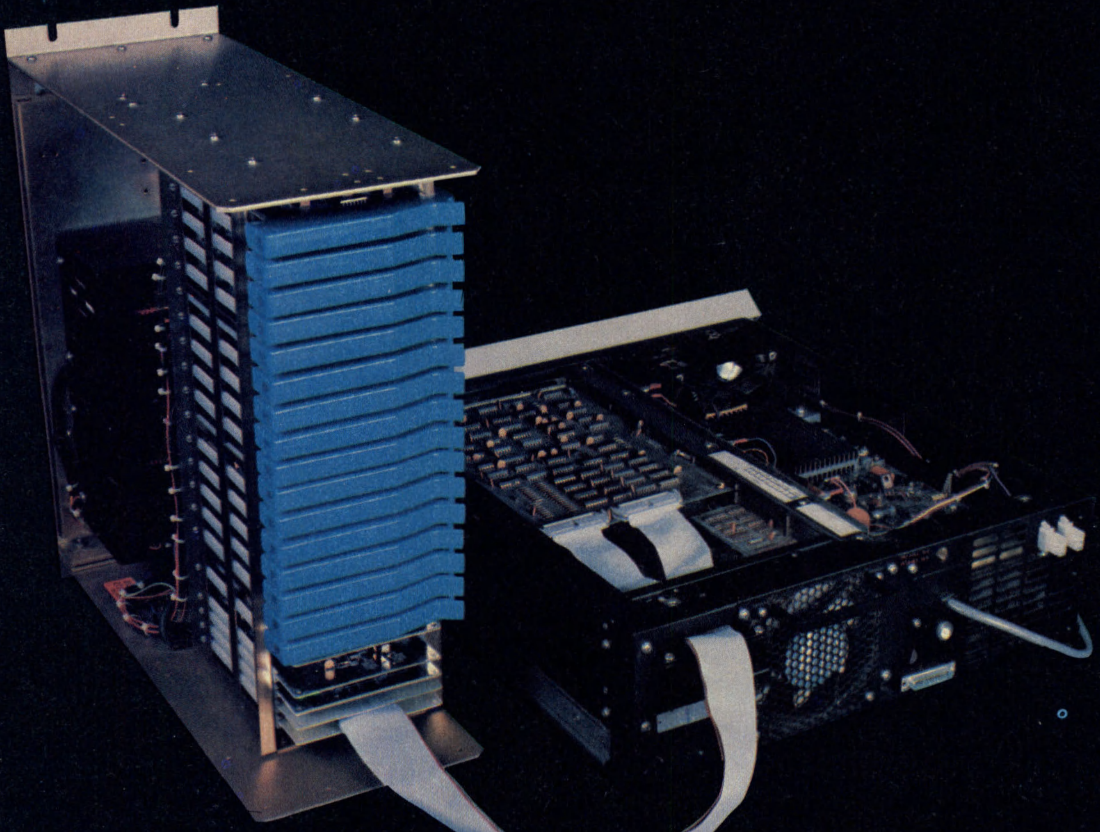

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The French Commissariat a l'Energie Atomique has recently developed a microprocessor based module intended to replace a minicomputer and cut in half the cost of Camac systems. Designated the JCAM-10, the module uses the Intel 8080 microprocessor and is three times as fast as a computer with the standard Camac interface. It reads and writes six times as fast as a Camac interfaced system. A full crate of Camac modules costs from $10,000 to $15,000, of which about 20% represents the overhead cost of the crate, power supply and control module. Suppliers of Camac modules include Kinetic Systems Corp., Columbia Scientific Industries, LeCroy Research Systems Corp., GEC-Elliot Process Instrumentation Ltd. and Dornier.

Hewlett-Packard Interface Bus. In 1972, Hewlett-Packard began publicizing the work it had underway to develop a scheme for interconnecting programmable instruments with each other and with computers. The key design goals for

★ The ability to delegate the control function to a device with control capability

★ Operation over a wide range of data rates, codes and configurations

★ Compatibility with a variety of measurement, stimulus, display, processor and storage products

★ Compatibility with many existing serial devices and convertibility to other interface methods.

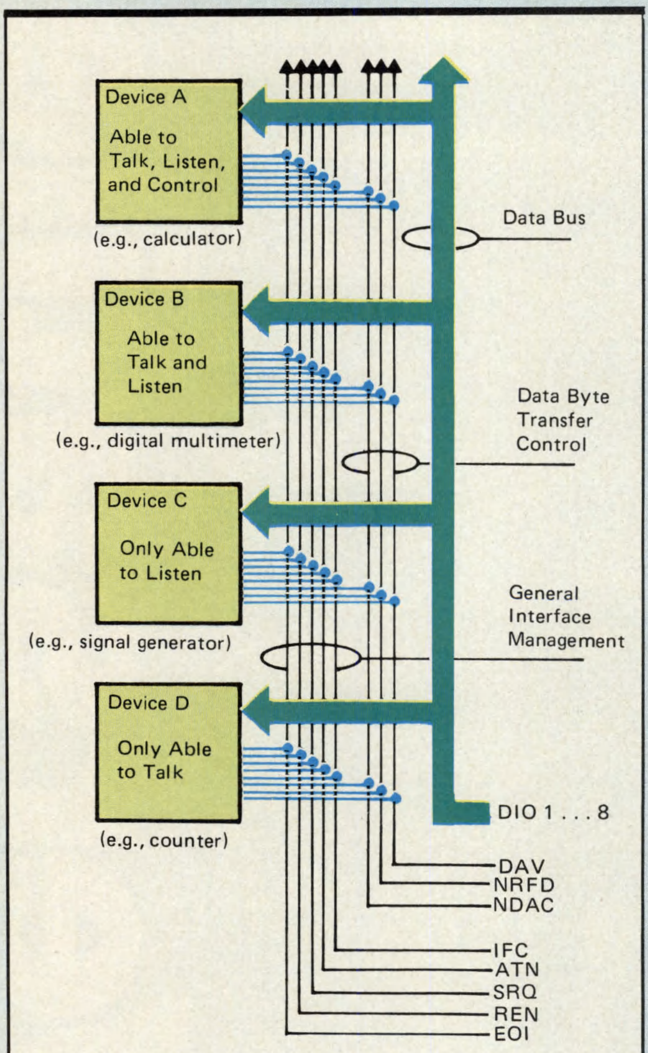

Fig 4 Hewlett-Packard's interface bus incorporates 16 signal lines, grouped into an 8-line data bus, a 3-line transfer bus and a 5-line interface management bus. In a typical system, devices can transmit data, receive data or perform both functions simultaneously.

The H-P interface bus was formally unveiled in October 1974; in mid-1975, the IEEE published its "Standard Dig tal Interface for Programmable Instrumentation", #488-1975, which is also based on the H-P interface bus. Obtain copies of the standard by writing IEEE at 345 E. 47 St., New York, NY 10017. Near the end of 1975, the American National Standards Institute (ANSI) accepted t IEEE standard as ANSI #MC.1-1975.

In recent months, Hewlett-Packard has expanded the i terface bus for use in data acquisition and control situations. The H-P 6940B multi-programmer, controlled by a programmable calculator through the standard interface, contains several plug-in analog and digital I/O cards for measurement, control and acquisition functions.

In the basic interface bus structure (Fig 4), a set of 16 signal lines interconnects several devices, each of which ha a different function. At any instant a device may merely monitor the activity on the bus or may function as a talker, listener or controller. A talker can transmit data to other devices via the bus and a listener can receive such data. Some devices can perform both roles (e.g., a programmable instrument can listen to receive its control instructions and talk to send its measurements). A typical system could include one element with a talker, listener and controller interface, such as a calculator, microprocessor or minicomputer; and a variety of other devices — talkers or listeners, or both.

The 16 signal lines within the bus appear in three sets. An eight-line data bus transfers data in bit-parallel, byte-serial form and also transfers certain commands. A 3-line transfer bus implements the handshaking process that synchronizes devices ready to transmit data with those ready to receive data. A 5-line interface management bus serves the controller.

manufacturing trends

Data acquisition subsystem design and usage is influenced by the type of signal to be sensed. In the laboratory, continuous and some batch manufacturing segments, analog inputs account for 72% of all applications. Digital inputs, contact closures, temperature and pressure switches and similar devices account for 28% of all inputs. Some batch and discrete manufacturing segments reverse these percentages. High-level analog inputs generally account for 20% of the inputs of a "typical" system, while low-level inputs account for the remaining 80%.

Temperature, flow, pressure and level units form the four types of sensors most frequently interfaced to data acquisition subsystems. All other types of analog sensors account for 13% of all inputs.

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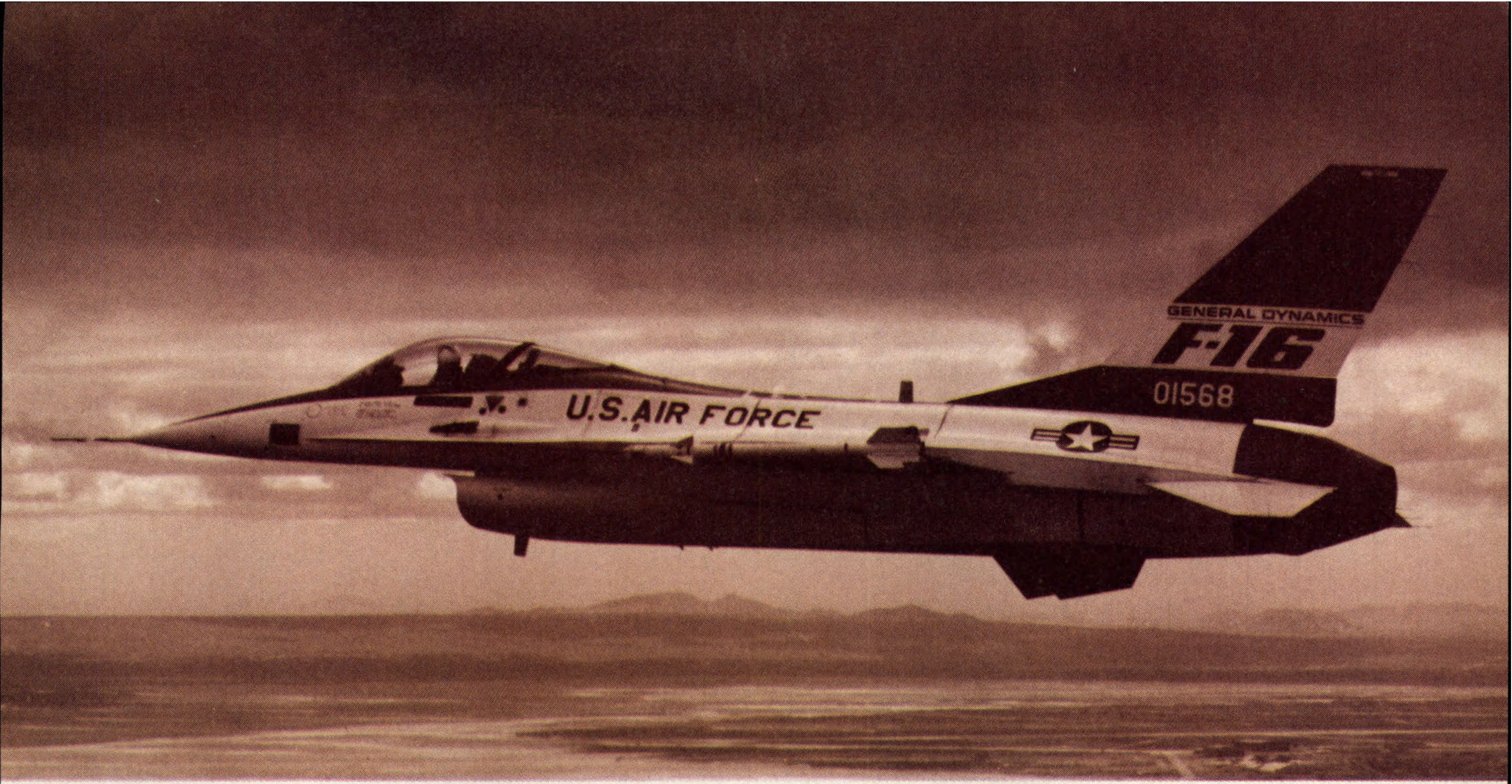

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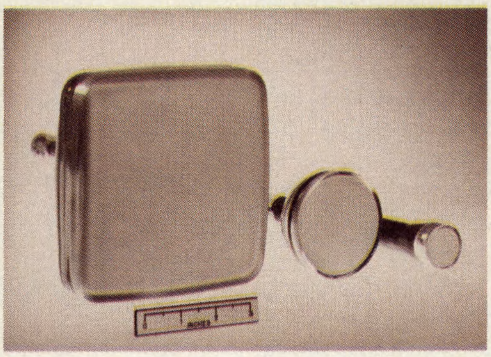

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Subsystem designers must target their product offerings to accommodate the elusive "typical" data acquisition system. The largest data acquisition systems have 1000 or more analog inputs, while a small system has 32 inputs or less. Our research indicates that the "typical" subsystem should be able to handle 256 analog inputs.

Inputs to a data acquisition subsystem can be either high level or low level. Low-level inputs are generally defined as less than 1 V full scale; full scale is usually 5 mV or 50 mV. High-level inputs are generally defined as 1 V full scale or greater. The typical subsystem should be able to handle 128 to 256 low-level analog inputs, and its high-level input signal handling capability should range from 0 to 64 channels. A subsystem that can handle 256 low-level inputs and 32 high-level inputs suits most applications.

Officials who set product policy for the design of data acquisition subsystems face a difficult task; they must produce a standard product that can serve a large number of customers with an even larger number of applications. Additionally, most subsystems find uses in a variety of one-of-a-kind applications and are unlikely to be sold in large volumes to a single customer.

The most timely and the most perplexing questions facing data acquisition subsystem manufacturers focus on the best method of designing intelligence into their products. Should they use minicomputers or microprocessors? If they use a microprocessor, which one should they use? We believe that the software support available for the chosen process often becomes the overriding consideration. Companies adept at designing data acquisition hardware are apt to bog down in the software development aspects of their intelligent subsystem projects. And data acquisition specialists, enamored with the microprocessor, often keep adding features until they have designed a computer that can handle analog data, rather than an intelligent data acquisition subsystem. The marketing, software and service problems that arise in the computer business are usually more than the data acquisition subsystem manufacturer can or wishes to handle.

Subsystem designers must also decide whether to add data communications capability to their products or leave that task to their customers. If they decide to add communications capability they must also decide whether to offer it in serial/2-wire form or in parallel form, and whether to provide interfaces to popular minicomputer I/O buses or to interface to an H-P or Camac bus. Finally, they must decide whether to offer signal conditioning or leave that task for their customers; if signal conditioning is offered, subsystem manufacturers must decide which sensors to handle.

Modular/PC board data acquisition systems make sense as part of a strategy designed to prevent the customer base developed by the module makers from yielding to IC manufacturers. By selling "higher level" subsystem modules containing ICs, the module manufacturers, and not their customers, become the OEM customers of the IC manufacturers. Such a strategy extends the evolutionary process that saw users of data acquisition components switch from standard components to modules and now to subsystem modules containing ICs.

But can any strategy successfully stop the IC manufacturers from penetrating the modular manufacturers' customer base? After all, in the digital area users switched from standard components, to modules, to IC flip-flops, to quad flip-flops, to MSI, and finally to RAMs, ROMs and microprocessors; there the IC manufacturers were not and could not be isolated from users.

We believe that the analog and quasi-digital world of data acquisition subsystems differs from the digital world:

★ Many users require assistance from module manufacturers
★ Analog circuits are more tricky to design than digital ones
★ The analog circuit designer and the digital circuit designer are different people, so the customer base is different
★ Analog module manufacturers have built their business by providing a level of application assistance not required of digital circuit manufacturers
★ Designing and building multichannel data acquisition systems and making them operate in noisy environments is difficult
★ The markets for data acquisition ICs are small compared with the markets for calculators, watches, microprocessors, RAMs and ROMs.

While the IC manufacturers have the financial, marketing, production and management resources to penetrate the data acquisition market, we believe that they will remain content serving as OEM suppliers to today's module manufacturers. We do not believe that the returns available to IC manufacturers as a result of penetrating data acquisition markets are nearly as attractive as the returns available in the digital areas with which they are more familiar. It does not appear sensible for IC manufacturers to choose to make a sizeable investment in data acquisition when they could achieve a much greater return in the digital area.

The module manufacturers that lack the resources to establish in-house thin-film, thick-film, bipolar or CMOS technologies and are fearful of the threat from the IC manufacturers have no choice but to enter the subsystem business to maintain their market share. As more functions are added to modules and ICs, and as "higher level" modules become even higher level "smart data acquisition subsystem" modules, these companies will grow more similar to systems houses. Those that are not fully integrated will become systems houses that build custom systems rather than standard products. This change will occur when the "higher level" modules become so complex that it is impossible to make them suitable for a large number of applications. ◆

The Full Story

The authors based this article on their 200-page report, "Data Acquisition Subsystems, 1976-1980." In addition to the information covered here, the report contains detailed information on market structures, user profiles and marketing considerations; it constitutes the second volume of a 3-volume series that also surveys data acquisition components and turnkey systems. Each volume costs $1500; all three sell for $3750. For more information, contact Venture Development Corp., One Washington St., Wellesley, MA 02181. (617) 237-5080

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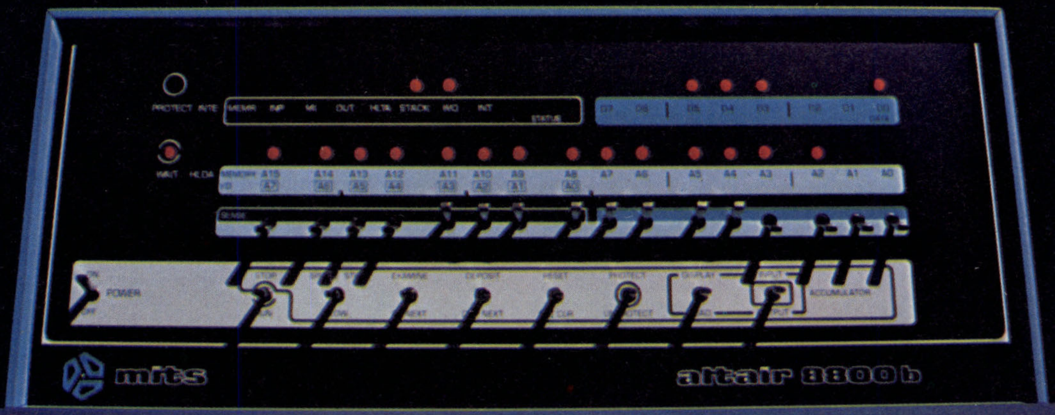
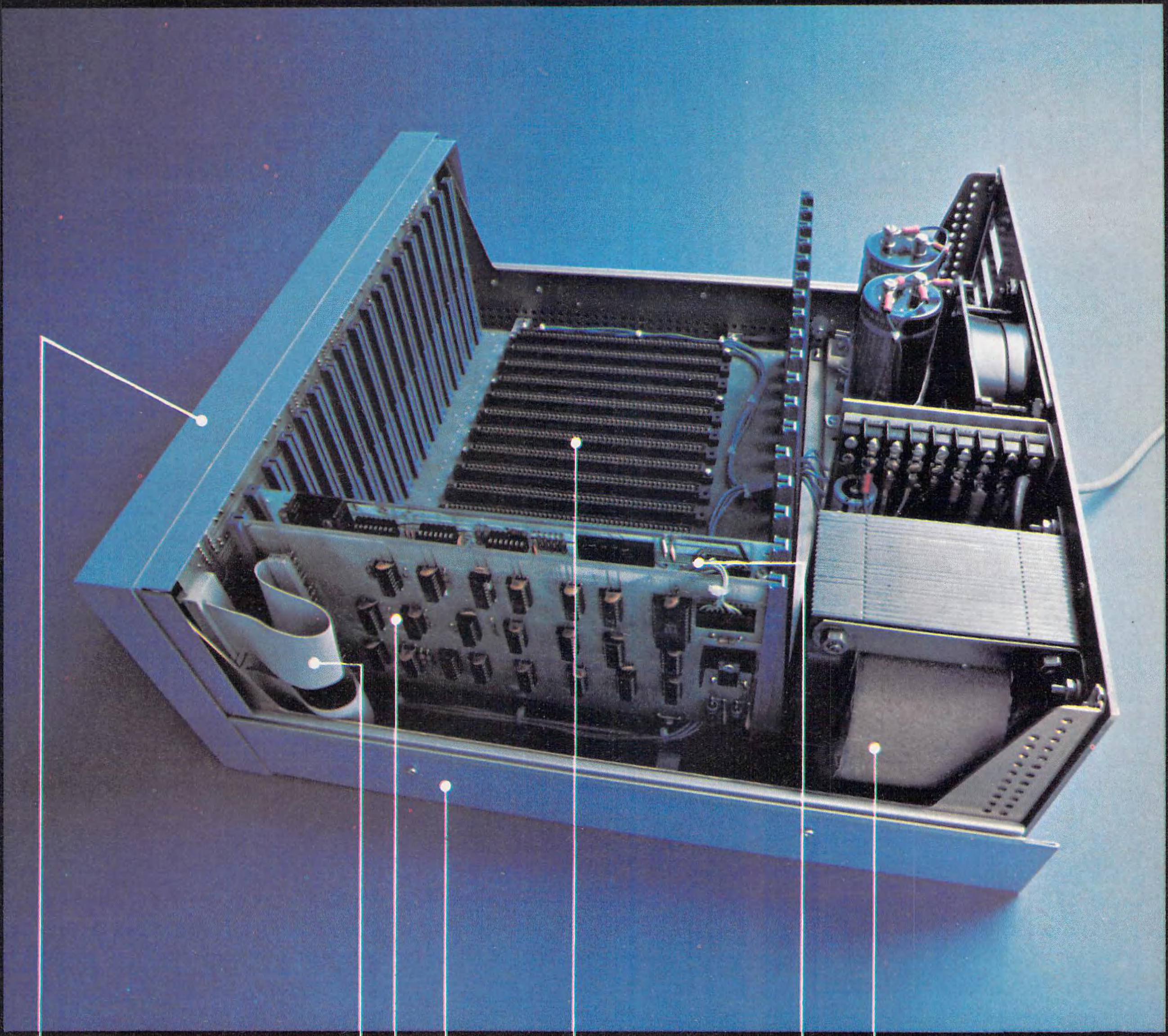
Introductory prices for the Altair 8800b are $840 for a kit with complete assembly instructions, and $1100 for an assembled unit. Complete documentation, membership into the Altair Users Club, subscription to "Computer Notes," access to the Altair Software Library, and a copy of Charles J. Sippl's Microcomputer Dictionary are included.





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CIRCLE 12

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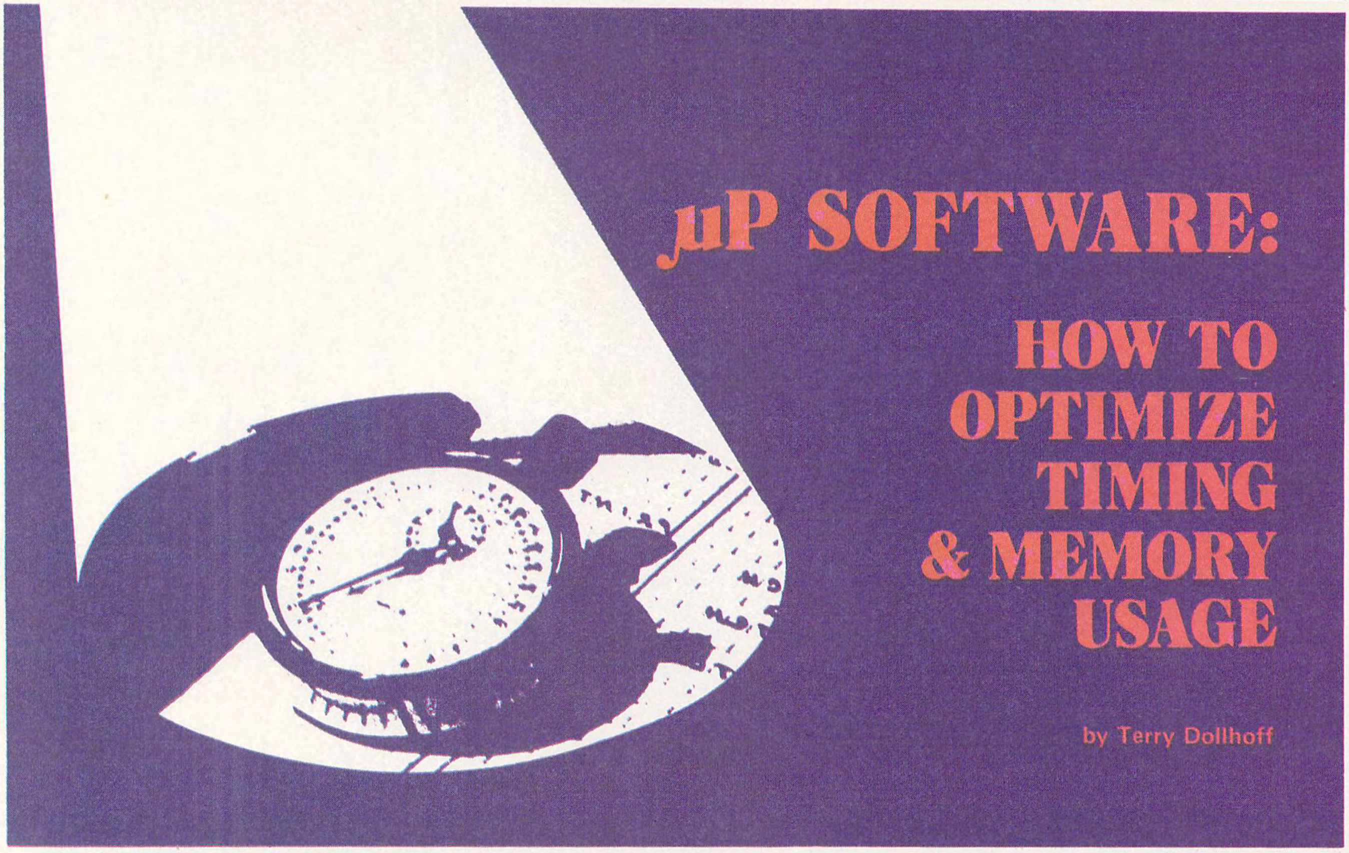
PART TWO: TECHNIQUES FOR THE TEXAS INSTRUMENTS TMS9900



µP SOFTWARE:

HOW TO OPTIMIZE TIMING & MEMORY USAGE

by Terry Dollhoff

Last month, I offered suggestions for optimizing timing and memory requirements in programs written for the Intel 8080 and the Motorola 6800. This month's programming tips focus on a 16-bit machine – Texas Instruments' 9900. The 9900 is not the first 16-bit microprocessor, but it is probably the most powerful one. Its architecture (Fig 1) is unlike most other 8- or 16-bit microprocessors'; the 9900 is identical to TI's 990 minicomputer.

You might think that the 9900 could replace other microprocessors because it is more powerful and easier to program. But alas, it too has drawbacks. First, it is word-oriented, a factor that often increases memory requirements. Second, it comes in a 64-pin package, which increases its cost.

architecture and addressing modes

The TI 9900 houses its 16 general registers (R0-R15) in memory; the only registers in the processor itself are a program counter, a status register and a pointer to the general registers. The program counter is a typical instruction address register, and the workspace pointer is a 16-bit register that holds the address of the first general register.

Fig 2 summarizes the 9900's instruction set. The first part of the figure provides the three least significant hexadecimal digits of each register operation instruction.

Computations in the 9900 can occur between the registers, between the registers and memory or between two memory locations. The processor always references a word because the least significant address bit is not available on an external pin. But internally, you can address either words (two consecutive bytes – the address of the first is even) or bytes. The microprocessor stores all instructions as consecutive words and has six possible addressing modes:

★ Immediate. The operand lies in the word following the instruction. For example,

```
        LI      R1,>1234        ;load R1 with 1234(hex)
```

loads register R1 with the hexadecimal value 1234. The '>' indicates a hexadecimal value to the assembler.

★ Register. The operand lies in one of the general registers, which in turn lie in memory. The address of register 'x' is WP+2*x, where WP denotes the contents of the workspace pointer. Be careful to preset WP at the beginning of your program; if you don't, the registers may be located on top of the program, a location that can cause serious problems.

★ Register indirect. The operand lies in the memory location whose address lies in one of the general registers. For example,

```
        MOV     *R1,R2          ;R2=(R1)
```

loads register R2 with the memory location whose address lies in R1.

★ Register indirect, auto increment. The operand lies in the memory location whose address lies in one of the general registers. After execution of the instruction, that general register is incremented by two. For example,

```
        MOV     *R1+,R2
```

loads register R2 with the memory location whose address lies in R1. After the move, R1 is incremented by two.

★ Indexed. The operand lies in the memory location whose address is a constant plus the contents of one of the general

Terry Dollhoff *is director of computer science at Acuity Systems, Inc., Reston, VA.*

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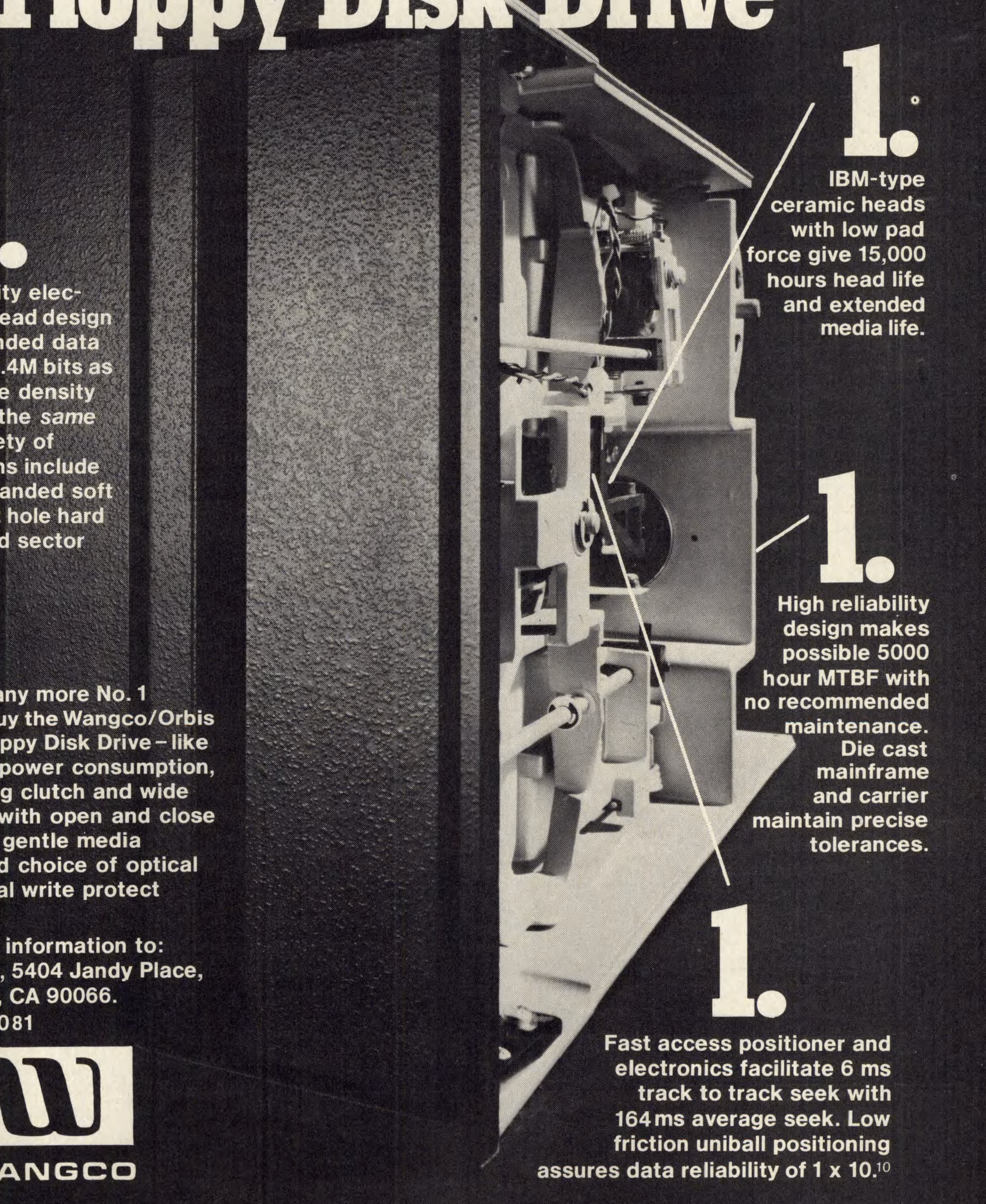

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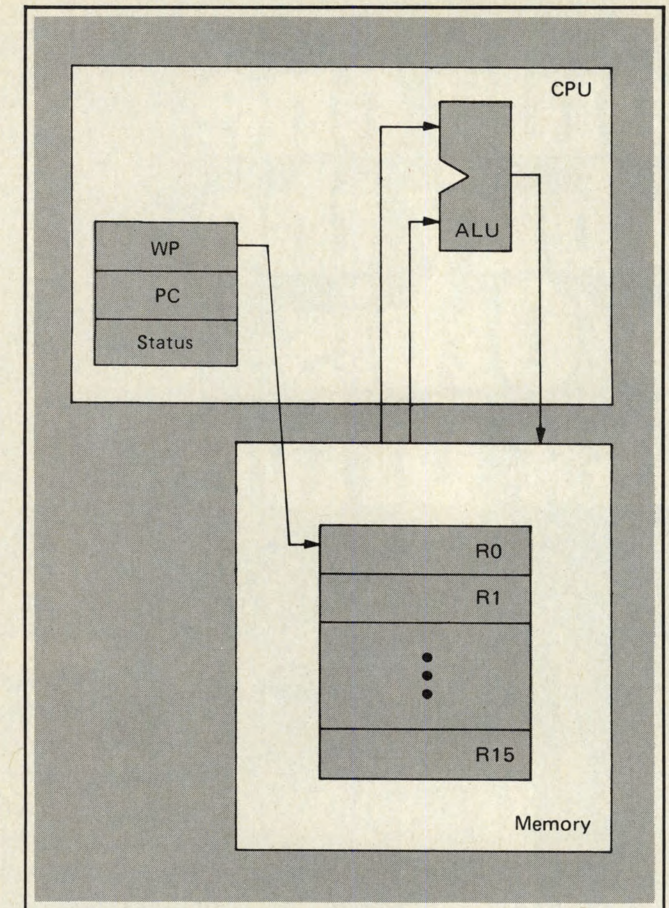

Fig 1 The Texas Instruments TMS9900, a 16-bit microprocessor, has architecture identical to the manufacturer's 990 minicomputer. Its 16 general registers (RO-R15) lie in memory; only a workspace pointer (WP), program counter (PC) and status register are housed in the processor. The workspace pointer, a 16-bit register, designates the first general register.

registers. If you use register R0, the operand is merely the constant. To move the contents of a variable, VAR, to register R1, use

```
        MOV     @VAR,R1
```

Because this instruction specifies no index register, the assembler assumes the R0 (no index) is desired. But

```
        MOV     @10(R1),R2
```

loads R2 with the memory location addressed by the contents of R1 plus 10.

★ Relative. Relative addressing can obtain the destination address for most of the 9900's jump instructions. To obtain the final destination address, you multiply the second byte of the instruction by two and add the result to the address of the next sequential instruction. The addition occurs in two's complement arithmetic, which lets you transfer control to an address ranging from -250 to +258 locations from the current instruction. Because all instructions are stored as words (two bytes), you can transfer control to a word within the range of -125 to +129 of the current instruction. An example of relative addressing is

```
        JMP     10
```

which transfers control to the address of the next sequential instruction plus 20 (10*2). If the jump occurred at >1200, it would transfer control to address >1214.

As you can see, the 9900's instruction set is more complicated than an average microprocessor's. Each of the opcodes is one word long, and if you use immediate, indirect or indexed addressing, the required constant lies in the word or words that follow the opcode. The constant for each source operand lies in the first word following the opcode, and the constant for the corresponding destination operand lies in the next available word. Thus, the 9900's instructions are one to three words (two to six bytes) long. This 6-byte instruction transfers the contents of variable VAR1 to VAR2:

```
        MOV     @VAR1,@VAR2     ;VAR2=VAR1
```

subroutine linkage

Unlike the 8080 and 6800, the 9900 doesn't use a stack to hold subroutine return addresses. Instead, it saves each return address in general register R11. For example, this instruction saves the address of BACK in R11 and transfers control to ROUT:

```
        BL      ROUT            ; call ROUT
BACK    .
        .
        .
```

To return from ROUT, code a jump to the contents of R11 (B *R11).

If one subroutine must call another, it must first save the contents of R11 and can achieve this result in several ways. The first – and simplest – method saves the return address in one of the general registers. For example, if a program calls ROUT, which must then call ROUT2, it could use this sequence:

```
        MOV     R11,R1          ; save return address
        BL      ROUT2           ; call next subroutine


        .
        .
        .

        B       *R1             ; exit
```

If your program has only two or three subroutine levels, this approach may be the most efficient one. But larger systems usually have too many subroutine levels to allow storage of all the return addresses in the registers. Such systems must save the return address in RAM, and one way to achieve that goal is to code

```
        MOV     R11,@TEMP       ; save return
```

To exit from the subroutine, use

```
        MOV     @TEMP,R11       ; get return
        B       *R11            ; exit
```

The major disadvantage of this technique is that it requires four words of instruction memory for the exit sequence, in addition to the word that holds the return address – a wasteful use of memory. If you always run the program in RAM (never put it in non-writeable storage), an alternate entry/exit sequence is

```
        MOV     R11,@EX+2       ; save return in exit branch

        .
        .
        .

EX      B       @0              ; exit
```

This sequence saves the return address in the second word of the branch instruction and thus eliminates the move. Its disadvantage is that the program modifies itself, so you can't place it in ROM. I would not normally recommend using any self-modifying techniques, but if you must write a quick-and-dirty routine and run it only from RAM, this approach works well.

You can save the return address another way – put it on a stack. Because of the microprocessor's addressing modes,

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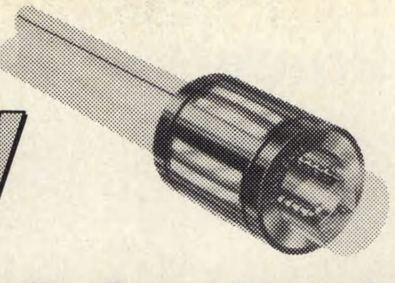

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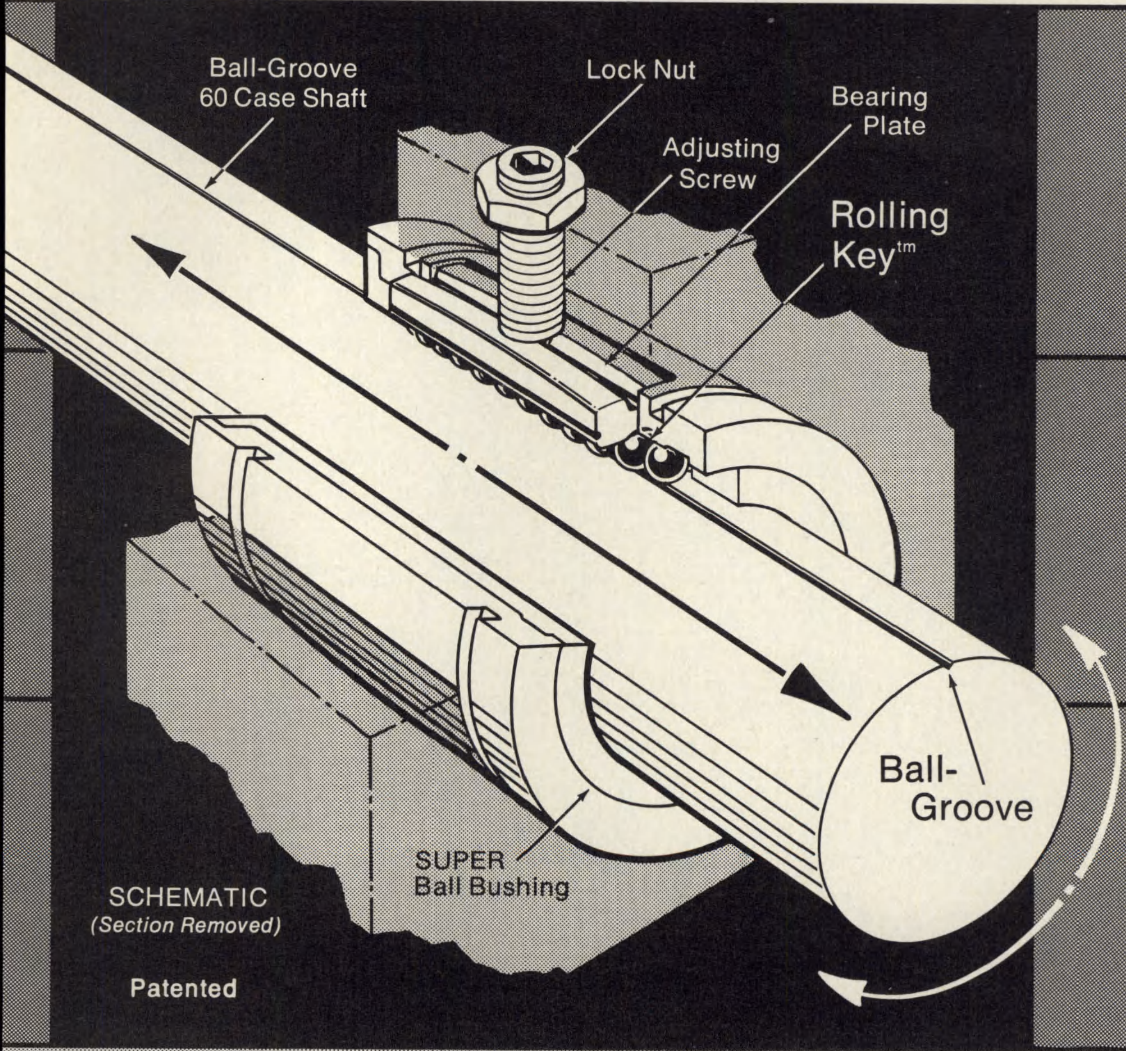
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Texas Instruments 9900 Instruction Set

		R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15		
xxxx	Rs,Rd	00s	04s	08s	0Cs	10s	14s	18s	1Cs	20s	24s	28s	2Cs	30s	34s	38s	3Cs	Rs,Rd	aaaa
	*Rs,Rd	01s	05s	09s	0Ds	11s	15s	19s	1Ds	21s	25s	29s	2Ds	31s	35s	39s	3Ds	*Rs,Rd	
	*Rs+,Rd	03s	07s	0Bs	0Fs	13s	17s	1Bs	1Fs	23s	27s	2Bs	2Fs	33s	37s	3Bs	3Fs	*Rs+,Rd	
	@Rs,Rd	02s	06s	0As	0Es	12s	16s	1As	1Es	22s	26s	2As	2Es	32s	36s	3As	3Es	@Rs,Rd	
	Rs,*Rd	40s	44s	48s	4Cs	50s	54s	58s	5Cs	60s	64s	68s	6Cs	70s	74s	78s	7Cs	Rs,Rd	bbbb
	*Rs,*Rd	41s	45s	49s	4Ds	51s	55s	59s	5Ds	61s	65s	69s	6Ds	71s	75s	79s	7Ds	*Rs,Rd	
	*Rs+,*Rd	43s	47s	4Bs	4Fs	53s	57s	5Bs	5Fs	63s	67s	6Bs	6Fs	73s	77s	7Bs	7Fs	*Rs+,Rd	
	@Rs,*Rd	42s	46s	4As	4Es	52s	56s	5As	5Es	62s	66s	6As	6Es	72s	76s	7As	7Es	@Rs,Rd	
	Rs,*Rd+	C0s	C4s	C8s	CCs	D0s	D4s	D8s	DCs	E0s	E4s	E8s	ECs	F0s	F4s	F8s	FCs	Rs,Rd	cccc
	*Rs,*Rd+	C1s	C5s	C9s	CDs	D1s	D5s	D9s	DDs	E1s	E5s	E9s	EDs	F1s	F5s	F9s	FDs	*Rs,Rd	
	*Rs+,*Rd+	C3s	C7s	CBs	CFs	D3s	D7s	DBs	DFs	E3s	E7s	EBs	EFs	F3s	F7s	FBs	FFs	*Rs+,Rd	
	@Rs,*Rd+	C2s	C6s	CAs	CEs	D2s	D6s	DAs	DEs	E2s	E6s	EAs	EEs	F2s	F6s	FAs	FEs	@Rs,Rd	
	Rs,@Rd	80s	84s	88s	8Cs	90s	94s	98s	9Cs	A0s	A4s	A8s	ACs	B0s	B4s	B8s	BCs	Rs,Rd	dddd
	*Rs,@Rd	81s	85s	89s	8Ds	91s	95s	99s	9Ds	A1s	A5s	A9s	ADs	B1s	B5s	B9s	BDs	*Rs,Rd	
	*Rs +,@Rd	83s	87s	8Bs	8Fs	93s	97s	9Bs	9Fs	A3s	A7s	ABs	AFs	B3s	B7s	BBs	BFs	*Rs+,Rd	
	@Rs,@Rd	82s	86s	8As	8Es	92s	96s	9As	9Es	A2s	A6s	AAs	AEs	B2s	B6s	BAs	BEs	@Rs,Rd	

A	Axxx	add Rs to Rd
AB	Bxxx	add Rs(byte) to Rd(byte)
AI	022s	add constant to Rs
ANDI	024s	AND constant with Rs
C	8xxx	compare Rs with Rd
CB	9xxx	compare Rs(byte) to Rd(byte)
CI	028s	compare constant with Rs
CKOF	03C0	clock-off
CKON	03A0	clock-on
COC	2aaa	compare (Rd and Rs) with Rs
CZC	2bbb	compare (Rd and Rs) with zero
DIV	3ccc	Rd=(Rd,Rd+1)/Rs,Rd+1=remainder
IDLE	0340	idle
JEQ	13yy	jump if equal
JGT	15yy	jump if greater than
JH	1Byy	jump if high
JHE	14yy	jump if high or equal
JL	1Ayy	jump if low
JLE	12yy	jump if low or equal
JLT	11yy	jump if less than
JMP	10yy	jump unconditional
JNC	17yy	jump if carry clear
JNE	16yy	jump if not equal
JNO	19yy	jump if no overflow
JOC	18yy	jump if carry set
JOP	1Cyy	jump if odd parity
LDCR	3aaa	d-bits of Rs to CRU

LI	020s	load Rs immediate
LIMI	0300	load interrupt mask immediate
LREX	03E0	load Rom and EXecute
LWPI	02E0	load workspace pointer immediate
MOV	Cxxx	move Rs to Rd
MOVB	Dxxx	move Rs(byte) to Rd(byte)
MPY	3ddd	(Rd,Rd+1)=Rd times Rs
ORI	026s	OR or constant with Rs
RSET	0360	reset
RTWP	0380	return with workspace
S	6xxx	subtract Rs from Rd
SB	7xxx	subtract Rs(byte) from Rd(byte)
SBO	1Dyy	set CRU bit yy
SBZ	1Eyy	set CRU bit yy
SLA	0Ans	shift Rs left (alg.) by n
SOC	Exxx	OR Rs with Rd
SOCB	Fxxx	OR Rs(byte) to Rd(byte)
SRA	08ns	shift Rs right(alg.) by n
SRC	0Bns	shift Rs right (circ.) by n
SRL	09ns	shift Rs right(log.) by n
STCR	3bbb	d-bits of CRU to Rs
STST	02Cs	Rs = status register
STWP	02As	Rs = workspace pointer
SZC	4xxx	Rd = Rd and not Rs
SZCB	5xxx	Rd(byte) = Rd(byte) and not Rs
TB	1Fyy	test CRU bit
XOP	2ccc	extended operation
XOR	2ddd	ex-OR Rs with Rd

	Rs	*Rs	*Rs+	@Rs	
ABS	074s	075s	077s	076s	absolute value of Rs
B	—	045s	047s	046s	branch
BL	—	069s	06Bs	06As	branch and link R11
BLWP	—	041s	043s	042s	branch and link workspace
CLR	04Cs	04Ds	04Fs	04Es	clear Rs
DEC	060s	061s	063s	062s	decrement Rs by one
DECT	064s	065s	067s	066s	decrement Rs by two
INC	058s	059s	05Bs	05As	increment Rs by one
INCT	05Cs	05Ds	05Fs	05Es	increment Rs by two
INV	054s	055s	057s	056s	invert Rs (ones comp.)
NEG	050s	051s	053s	052s	negate Rs (twos comp.)
SETO	070s	071s	073s	072s	set Rs to ones
SWPB	06Cs	06Ds	06Fs	06Es	swap bytes of Rs
X	048s	049s	04Bs	04As	execute inst. at Rs

Fig 2 Clip and save this summary of the 9900's instruction set. The top portion of the summary provides the three least significant hexadecimal digits of each register operation instruction.

creating such a software stack is simple. During the program's initial start, load one of the general registers, say R15, with the address of the stack's first location. Then you can place an entry on the stack this way:

```
        MOV     R11,*R15+           ; stack R11
```

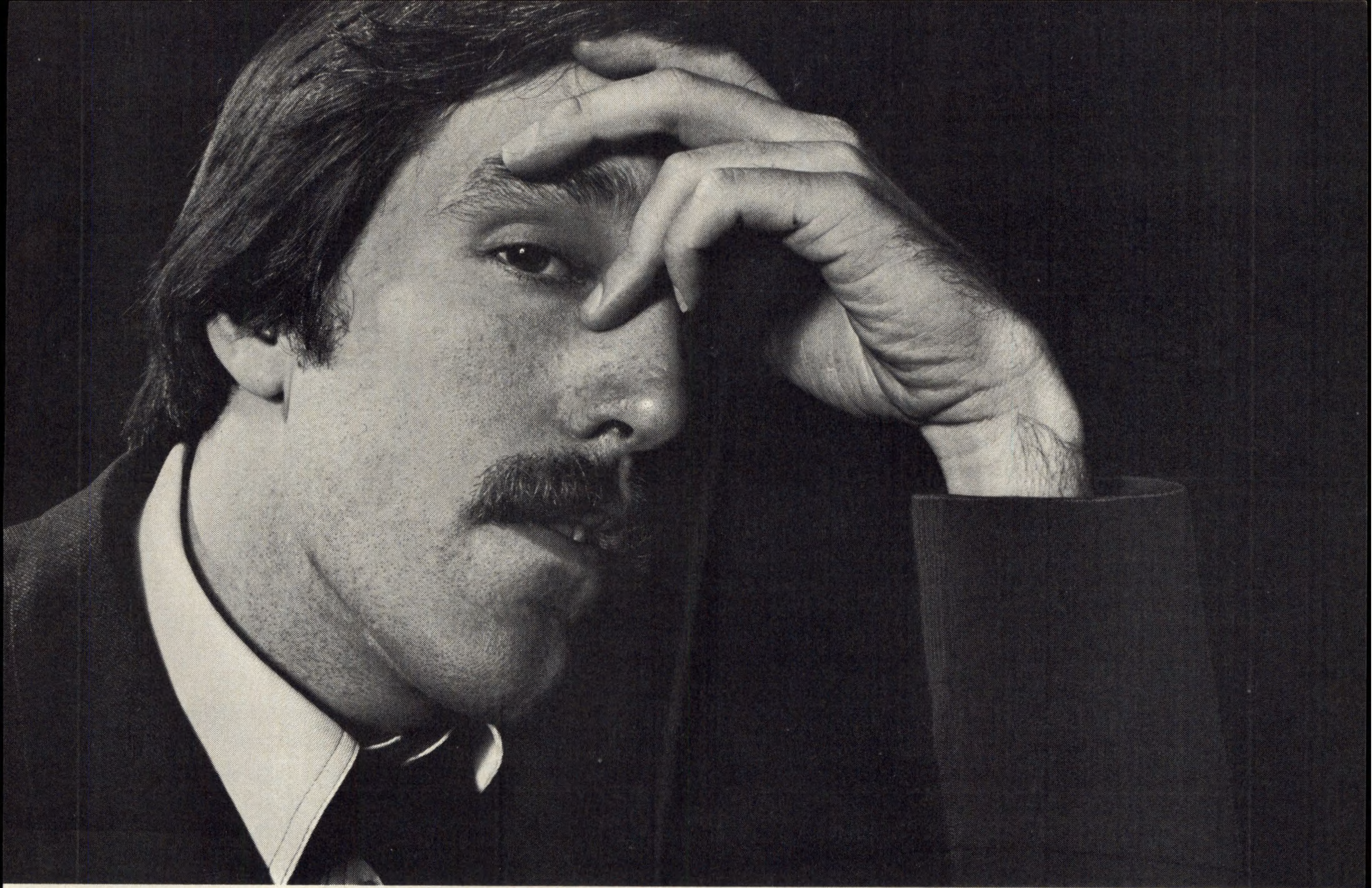
The stack pointer increments after the store, so the stack builds up instead of down as in other microprocessors. Retrieving an entry from the stack requires two instructions:

```
        DECT    R15                 ;R15=R15-2
        MOV     *R15,R11            ; get the top entry
```

A stack can also save some of the other general registers used by the subroutine. If the subroutine requires several registers, another approach uses the Branch and Link Workspace Pointer (BLWP). This instruction is also a subroutine call, but before execution it resets the workspace pointer, an action that gives the subroutine a whole new set of registers to work with – without having to store the old ones. This instruction is valuable, but use it with discretion because it requires additional memory – both for the call and for the new set of registers (16 words).

passing parameters and returning results

Last month I discussed several methods for passing data to subroutines – data that resides in a register or following a subroutine call, or addresses that follow the subroutine call. Because the return address of a routine resides in one



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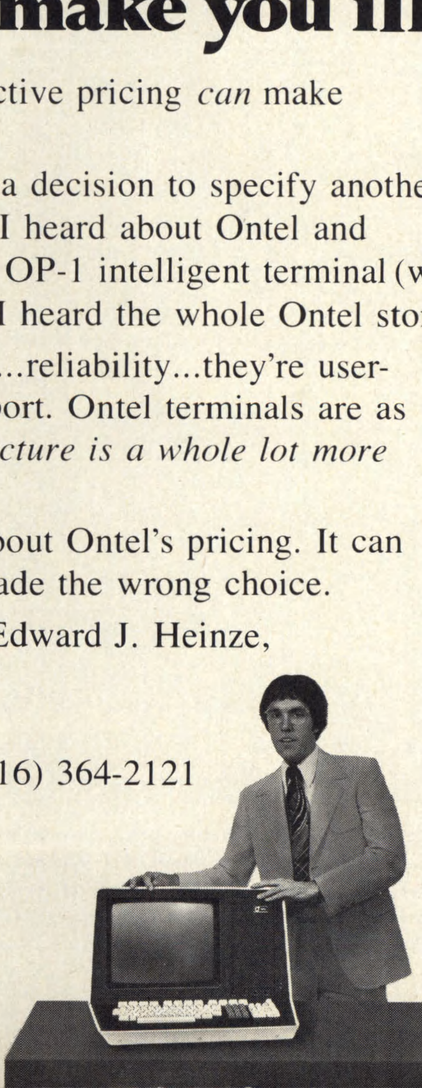

of the 9900's general registers, passing parameters or their addresses following a call is an especially useful procedure in this microprocessor. For example, last month I discussed a set of floating point routines – FADD, FDIV, FMUL and FSUB. Each routine requires three parameters, the addresses of which occur after the subroutine call. If you use the same approach with the 9900, this sequence can calculate X1=X2*X3+X4:

```
BL      @FMUL        ;TMP=X2*X3
DATA    X2
DATA    X3
DATA    TMP
BL      @FADD        ;X1=TMP+X4
DATA    TMP
DATA    X4
DATA    X1
```

Before you can manipulate the parameters, you must place them in the registers with this sequence:

```
MOV     *R11+,R1     ;R1=address of param1
MOV     *R11+,R2     ;R2=address of param2
MOV     *R11+,R3     ;R3=address of param3
```

Notice how the indirect-with-auto-increment addressing mode avoids the need for intermediate increments.

Many subroutines must return results to their calling programs. The easiers way to achieve this goal is to return the result in one of the general registers – a procedure that works fine if you call the subroutine via a BL instruction. But if you use BLWP or the yet-to-be-discussed XOP instruction, the calling routine uses a different set of registers than the subroutine. So if you place the results in the registers, they will be lost when control returns to the calling program and the workspace pointer is reset. Because the 9900's registers lie in memory, you can deal with this problem simply.

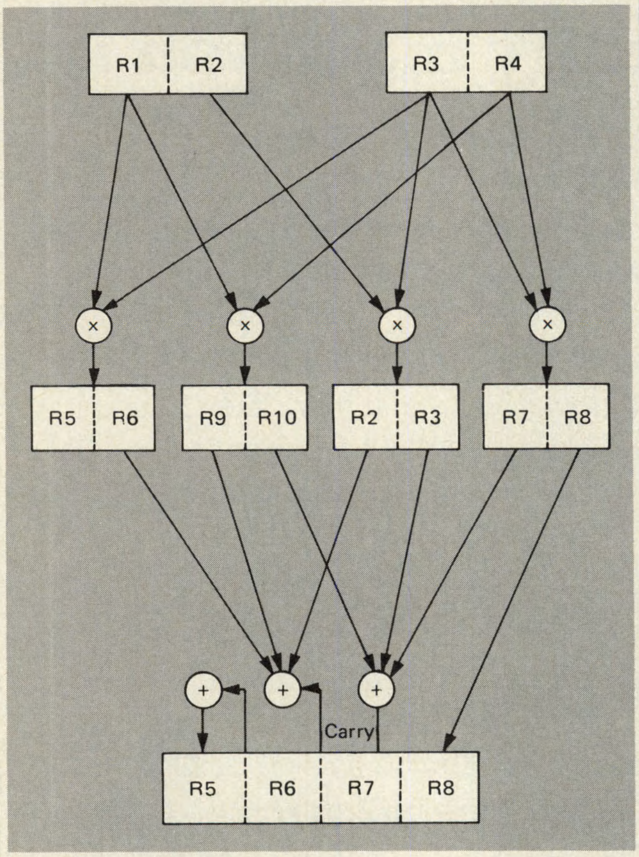

Fig 3 To perform a double precision multiply operation on two unsigned 32-bit numbers, you can use four single precision multiplies combined according to "cross multiply" techniques. Coding for the operation appears in Listing 4.

Assume you want to return a value in R0 and R1 – the old workspace. When the microprocessor executes BLWP, it saves the old workspace pointer in R13. Using this fact, you can create a sequence to store values in the previous workspace:

```
MOV     R0,*R13        ;old R0=new R0
MOV     R1,@2(R13)     ;old R1=new R1
```

The old register "i" is the same as memory location R13+2*i and you can address that location by @i+i(R13). R0 is a special case, because @0(R13) is the same as *R13.

byte-oriented, BCD and extended operations

Although the 9900 is primarily a 16-bit processor, it can also handle most byte operations, which, however, may have a few confusing aspects. First, whenever you address a register in the byte mode, the microprocessor uses the left byte of the register (not the right byte as you would expect – and as would be more convenient). Second, whenever the processor references memory, it reads a full word and selects the proper byte of that word internally. Thus, it isn't necessary for the processor to supply the external memory addressing circuitry with the least significant address bit – so it doesn't. This is why the processor has only 15 address bits. Overlooking these minor byte-addressing quirks, you'll quickly discover that the 9900 can cope with byte operands nearly as well as it can with full word operands. To add the contents of byte B1 to B2, for example, use

```
AB      @B1,@B2        ;B2=B2+B1
```

The TI 9900 has no BCD operations – that is, no decimal adjust operation. Nevertheless, you may require a BCD representation for I/O. Here's a routine to convert R1 to a BCD number in R3:

```
        LI      R0,4         ;R0=digit count
LOOP    MOV     R1,R2        ;left (R1,R2)=value
        CLR     R1
        DIV     @TEN,R1      ;R1=value, R2=digit
        SLA     R2,12        ;reposition digit
        SRL     R3,4         ;make room
        A       R2,R3        ;add in
        DEC     R0           ;continue until done
        JNE     LOOP
TEN     DATA    10           ;constant
```

Remember the 8080 restarts and the 6800 software interrupt I discussed last month? The 9900 offers a similar instruction, termed Extended Operation (XOP), which you can use in the same manner as a restart or software interrupt but which allows you to pass parameters. The XOP execution resembles that of BLWP, but the target address is determined by the XOP transfer vectors. Sixteen possible XOPs exist, and the source operand goes to R11 of the new workspace. For example,

```
XOP     @x,15
```

performs an extended operation 15 and places the contents of variable x in the new R11. The workspace pointer and address for extended operation 15 lie in memory locations

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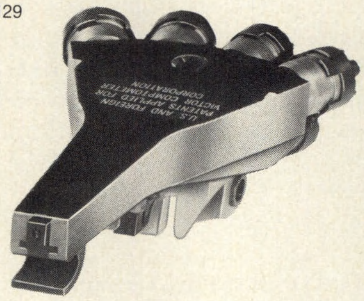

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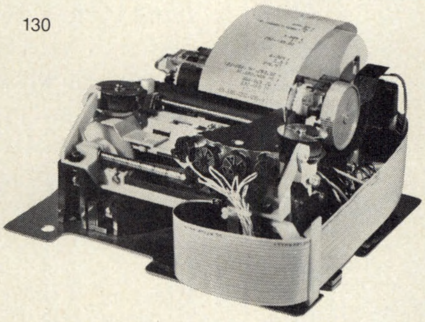

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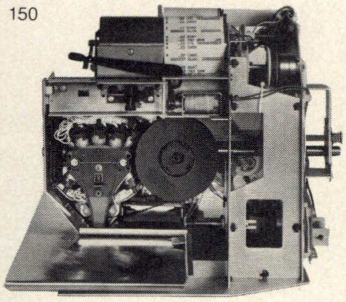

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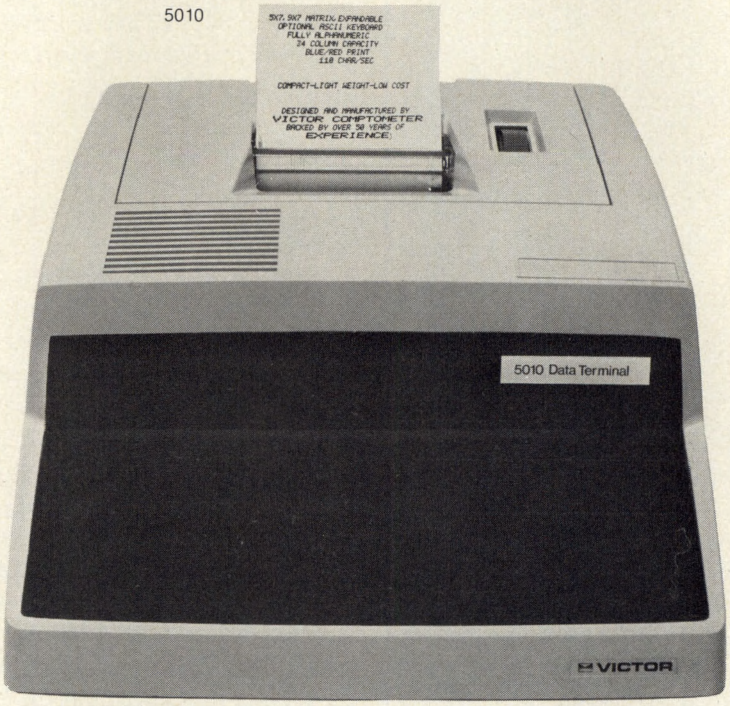
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Listing 1. Sequence That Calculates X3=X1*X2

```
        MOV     @X1,R1      ;R1=X1
        MOV     @X2,R3      ;R3=X2
        MOV     R1,R2       ;R2(sign)=sign of X1*X2
        XOR     R3,R2
        ABS     R1          ; get rid of signs
        ABS     R3
        MOV     R2,R2       ; test sign
        MPY     R3,R1       ;(R1,R2)=X1*X2
        JGT     GO          ;jump if product is plus
        NEG     R2          ;R2=X1*X2 (lower 16 bits)
GO      MOV     R2,@X3
```

Listing 2. Sequence That Calculates X3=X1/X2

```
        MOV     @X1,R2      ;R2=X1
        MOV     @X2,R3      ;R3=X2
        MOV     R2,R4       ;R4(sign)=sign of X1/X2
        XOR     R3,R4
        ABS     R2          ;get rid of sign
        ABS     R3
        CLR     R1          ;clear R1 (upper bits of
                             numerator
        DIV     R3,R1       ;R1=(R1,R2)/R3
        MOV     R4,R4       ; test sign
        JGT     GO          ; correct if minus
        NEG     R1
GO      .
        .
        .
```

Listing 3. Sequence For Full Divide Capability

```
        MOV     @X1,R1      ;(R1,R2)=X1
        MOV     @X1+2,R2
        MOV     @X2,R3      ;R3=X2
        MOV     R1,R4       ; calc. sign
        XOR     R3,R4
        ABS     R3          ;get rid of sign of X2
        ABS     R1          ;get rid of sign of X1
        JGT     L1          ; if X1 was minus, invert
                             lower half
        ABS     R2
        JNE     L1          ; if R2≠0 readjust R1
        DEC     R1
L1      DIV     R1,R3       ; divide
        MOV     R4,R4       ; test sign of result
        JGT     G0          ; correct if minus
        NEG     R1
GO      .
        .
        .
```

7C through 7F. For other extended operations, the extended operation transfer vector lies in location >40+i*4 through >40+(i+1)*4-1.

hardware multiply/divide

Although the 9900's hareware multiply and divide instructions are useful, they have one idiosyncracy – they require unsigned operands. This requirement is unfortunate, because the rest of the processor uses normal two's complement operands. All is not lost, however, because you can easily form a signed two's complement multiply. If X1 and X2 are two arbitrary numbers, then X1*X2's sign is the exclusive OR of the signs of X1 and X2. Capitalizing on this idea, the sequence in Listing 1 calculates X3=X1*X2.

The multiply operation produces a 32-bit result (stored in R1,R2 for the example in Listing 1) but does not affect any of the condition bits (that's why the test can be performed before the multiply). After the multiply the sequence converts the result back to two's complement form. Because you will probably use the result for some further add or subtract operation, only the lower word of the product is converted; converting both words is a more difficult task. This sequence won't work:

```
        NEG     R2
        NEG     R3
```

Why not? If R2=1 and R3=1, then the two's complement of (R2,R3) is >FEFF. But the two's complement of 1 is >FF, so this faulty sequence yields >FFFF instead of the required >FEFF. The proper sequence takes the one's complement of R2 except when R3=0:

```
        INV     R2          ;R2=one's comp. of R2
        NEG     R3          ;R3=-R3
        JNE     ZRO         ; if R3=0, adjust R2
        INC     R2          ;R2=two's comp. of R2
ZRO     .
        .
```

You can use a similar approach to construct a signed divide. The sign of X1/X2 is the exclusive OR of X1,X2. If X1 and X2 are both 16-bit two's complement variables, then the routine in Listing 2 calculates X1/X2.

In Listing 2, DIV divides a 32-bit operand by a 16-bit operand. Because the example uses a 16-bit operand, that operand goes to the lower register of the pair of registers, and the sequence clears the upper register. If you require full divide capability, recode the routine as in Listing 3.

Though the multiply is restricted to integer operands, you can also use it to perform fractional operations – an approach termed scaling. Here's a simple example. If the decimal point of X1 occurs at the extreme right and the decimal point of X2 occurs at the extreme left, then the decimal point of X1*X2 occurs between the two registers. Using this approach, you can multiply ABC by 0.75:

```
CON     DATA    >C000       ; constant of 0.75 (decimal
                              at left)
        MOV     @ABC,R1     ;get operand
        MPY     @CON,R1     ;(R1=integer part, R2=
                              fraction part)
```

Multiplies in the 9900 are unsigned, but you can turn this "defect" into an asset. For example, suppose you must create a double precision multiply (32 bits times 32 bits). If you consider unsigned numbers only (handle signs as in the previous examples), you can form a 32-bit multiply (which produces a 64-bit result) using four single precision multiplies (Fig 3). The approach uses what are commonly called "cross multiply" techniques. But before considering the double prescision multiply, look at the double precision add, which forms an integral part of the multiply routine. To calculate (R1,R2)=(R1,R2) + (R3,R4), use this coding (assume all values are unsigned):

```
            A       R4,R2       ; add lower half
            JNC     L1          ; if Cy, correct upper
            INC     R1
L1          A       R3,R1       ; add upper half
```

Using this same concept for the addition, you can create the 32-bit multiply routine shown in Listing 4.

signal processing applications

The TI 9900's advanced instruction set and TI's announcement that a higher-speed I^2L processor will appear next year both presage a new set of microprocessor applications in signal processing. Because of the required mathematics, most off-the-shelf microprocessors can't handle most signal processing tasks, but the 9900 can tackle a few of them.

Most signal processing algorithms use the Sin, Cos, or other trigonometric functions as an integral part of the filter computation. So I devote this month's discussion of arithmetic optimization to a trigonometric algorithm – one ideally suited to the 9900.

The CORDIC (COordinate Rotation DIgital Computer) algorithm is the same one used in many hand calculators. It relies on a few mathematical facts. First, any given angle in the 0-90° range can be represented as a sum or difference of a set of base angles:

$A = \Sigma d_i a_i$ where $d_i = \pm 1$

a_i = base angle.

This identity isn't true for any random selection of base angles, but you can see that 90°, 45°, 22.5°, . . . forms one

Listing 4. 32-Bit Multiply Routine

```
        MOV     R1,R5       ; R5,R6=R1*R3
        MPY     R3,R5
        MOV     R2,R7       ; R7,R8=R2*R4
        MPY     R4,R7
        MOV     R1,R9       ; R9,R10=R1*R4
        MPY     R4,R9
        MPY     R2,R3       ; R3,R4=R2*R3
        CLR     R0          ; R0=carry accumulator
        A       R3,R7
        JNC     L1
        INC     R0
L1      A       R10,R7
        JNC     L2
        INC     R0
L2      CLR     R1          ; R1=carry accumulator
        A       R2,R6
        JNC     L3
        INC     R1
L3      A       R9,R6
        JNC     L4
        INC     R1
L4      A       R0,R6       ; add-in carry
        JNC     L5
        INC     R1
L5      A       R1,R5       ; add-in other carry
```

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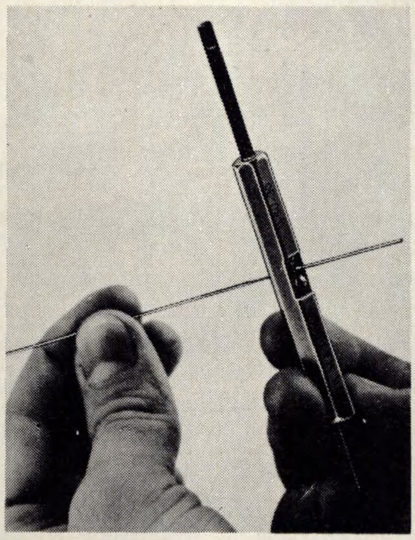
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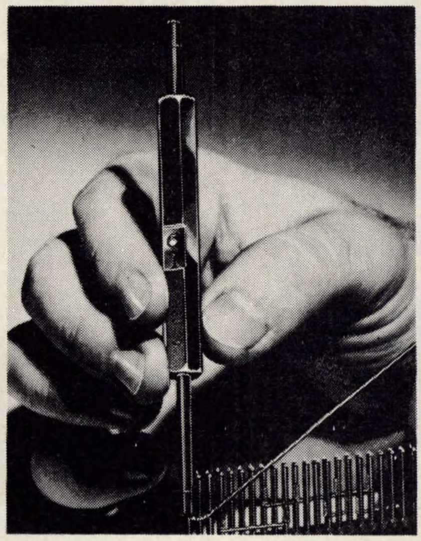
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Listing 5. Sine And Cosine Calculations

```
*
* This program will calculate the
* Sin and Cos of an angle v
* on entry, R1=v*256
* on exit, R2=sin, R3=cos
CORD  CLR    R2              ; x=0
      LI     R3, 19898       ; y=6072526*32768
                                           (2**15)
      CLR    R4              ; xo=0
      MOV    R3,R5           ; yo=y
      CLR    R0              ; shift=0
      CLR    R6              ; count=0
      NEG    R1              ; v=-v
LOOP  MOV    R1,R1           ; test sign(v)
      JLT    L10             ; jump if minus
      S      R5,R2           ; x=x-y/2**i
      A      R4,R3           ; y=y+x/2**i
      S      @TAB(R6),R1     ; v=v-ATan(1/2**i)
      JMP    L20
L10   A      R5,R2           ; x=x+y/2**i
      S      R4,R3           ; y=y-x/2**i
      A      @TAB(R6),R1     ; v=v+ATan(1/2**i)
L20   INC    R0              ; update shift/count
      INCT   R6
      MOV    R2,R4           ; set R4=x/2**i
      SRA    R4,R0
      MOV    R3,R5           ; set R5=y/2**i
      SRA    R5,R0
      CI     R0,12           ; cont. for 12 iter.
      JNE    LOOP
      B      *R11            ; return to caller
*
* Table of Arctangents
*
TAB   DATA 11520             ; ATan(1/)*256
      DATA 6800              ; ATan(1/2)*256
      DATA 3593              ; ATan(1/4)*256
      DATA 1824              ; ATan(1/8)*256
      DATA 916               ; ATan(1/16)*256
      DATA 458               ; ATan(1/32)*256
      DATA 229               ; ATan(1/64)*256
      DATA 115               ; ATan(1/128)*256
      DATA 57                ; ATan(1/256)*256
      DATA 29                ; ATan(1/512)*256
      DATA 14                ; ATan(1/1024)*256
      DATA 7                 ; ATan(1/2048)*256
```

possible base set. The second cornerstone of CORDIC is a pair of trigonometric identities:

$$\text{Sin}(a+b) = [\text{Sin}(a) + \text{Tan}(b)\text{Cos}(a)]\,\text{Cos}(b)$$
$$\text{Cos}(a+b) = [\text{Cos}(a) - \text{Tan}(b)\text{Sin}(a)]\,\text{Cos}(b)$$

If you represent a given angle as a sum or difference of a set of as-yet unspecified base angles, you can calculate the Sin and Cos of that angle by first calculating

$$X_0 = 0$$
$$Y_0 = 1$$
$$X_i = X_{i-1} + \text{Tan}(d_i a_i)*Y_{i-1}$$
$$Y_i = Y_{i-1} - \text{Tan}(d_i a_i)*X_{i-1}$$

This procedure produces $X_n = R_n\ \text{Sin}(\theta)$ and $Y_n = R_n\ \text{Cos}(\theta)$, where Rn is $1/(\text{Cos}(d_i a_i)* \ldots *(\text{Cos}(d_n a_n))$. So far there's nothing to cheer about, because the algorithm involves many more multiplies than a simple Taylor series. But the plot thickens. If you define the base angles as

$$a_i = \text{Tan}^{-1}(1/2^{i-1})$$

then

$$\text{Tan}(a_i) = 1/2^{i-1}$$

This definition lets you reduce all of the multiply operations to a right shift. Using the base angles as defined, you can restate the algorithm:

$$V_0 = -\theta$$
$$X_0 = 0$$
$$Y_0 = 1/Rn\text{-}0.60725$$
$$X_i = X_{i-1} - \text{SIGN}\ (V_{i-1})*Y_{i-1}/2^{i-1}$$
$$Y_i = Y_{i-1} + \text{SIGN}(V_{i-1})*X_{i-1}/2^{i-1}$$
$$V_i = V_{i-1} - \text{SIGN}\ (V_{i-1})*(\text{ATAN}(1/2^{i-1}))$$

If you store the ArcTan values in a table, this algorithm requires only shift, add and subtract operations. The shift operation requires a variable shift constant, which is why the 9900 suits the algorithm. If you store the shift count in R0, one instruction can perform the variable shift:

```
SRA     R1,R0          ; shift R1 right by (R0)
```

Because the Sin and Cos are fractional values, you must scale the input to the routine. To keep matters simple, scale the angle so that R1=angle*256, an operation that provides 8 bits of integer and 8 bits of fraction. Scale the X,Y values so that X=SIN*32768 and Y=COS*32768, an operation that provides 16 bits of signed fraction. In the complete algorithm (Listing 5) the input angle lies in R1 and the outputs lie in R2 and R3. The subroutine calculates both the Sin and Cos, and you can calculate the Tan by one additional divide.

getting started

How does a novice microprocessor user begin designing? After arming yourself with books on your microprocessor and algorithms to try, how do you try them? I recommend purchasing an evaluation kit and performing some experiments. Program several simple subroutines like the ones I've developed here. I don't recommend starting cold and attempting to program your application, a procedure that forces you to get the job done rather than learn about the processor. If you take the time to learn about the processor, you'll eventually have a job that's well done, not just done.

If you use the Intel 8080 or Motorola 6800, you can obtain the manufacturers' evaluation kits – just add a TTY or RS 232 terminal and off you go. If you use the TI 9900, your range of selection is much smaller because the processor is still very new. TI doesn't yet offer an evaluation kit; the only TI 9900 evaluation kit I know of is offered by Technico, Inc., a TI distributor in the Baltimore area.

Next month, Dollhoff will continue his exploration of microprocessor software optimization and will focus on the Fairchild F8. ◆

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Density, power, clocking tradeoffs favor 16-pin 4K RAMS in small systems

While 22-pin 4K RAMs dominate semiconductor mainframe-memory design, neither the 16-pin nor the 18-pin package has established a similar edge as the preferred 4K RAM style for smaller (especially microprocessor based) digital systems. This confusion has developed because neither pinout style possesses decisive design advantages or prohibitive drawbacks; the tradeoffs have proved roughly equal. Sixteen-pin 4K RAMs, for example, allow the high packing density required by most microprocessor based systems – they are 36% smaller than 22-pin packages. But they also demand more multiplexing capability than their 18-pin rivals. Eighteen-pin 4K RAMs, by contrast, avoid some pin-sharing and its resulting complexity but require more complex timing capabilities than 16-pin units.

Dave House, applications manager at Intel Corp., Santa Clara, CA, has compared the strengths and weaknesses of 16- and 18-pin 4K RAMs to determine their relative effectiveness in small digital systems. He concludes that 16-pin devices offer more advantages in microprocessor based designs than their 18-pin counterparts, but he cautions that in about two years both contenders will yield to 16-pin 16K RAMs.

4K-RAM PIN ASSIGNMENTS

16-PIN	18-PIN
22 Pins (Basic 4K)	22 Pins (Basic 4K)
- 6 Pins for Addresses	- 1 Pin for 5V Supply
+1 Pin for Second Clock	- 1 Pin for Chip Select
- 1 Pin for No Connect	- 1 Pin for Multiplexed I/O
	- 1 Pin for No Connect
16	18

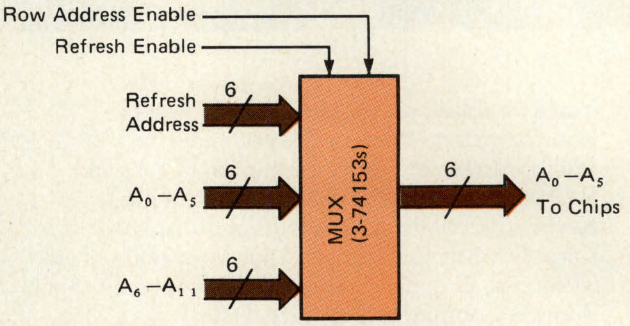
House first examines address multiplexing tradeoffs in the two designs. The 16-pin units perform this task while the 18-pin devices don't. So a 16-pin part requires a second multiplexer in addition to the 6-bit multiplexer it uses for refresh addresses. Together, these two multiplexers occupy three TTL-MOS integrated circuits, whereas the first multiplexer alone requires only two such ICs.

To control that extra multiplexer, a 16-pin 4K RAM requires a tap on a delay line or half of a 9602 dual one-shot multivibrator. Either of these components produces a level transition 100-125 ns after the falling edge of the RAM's $\overline{RAS}$ signal.

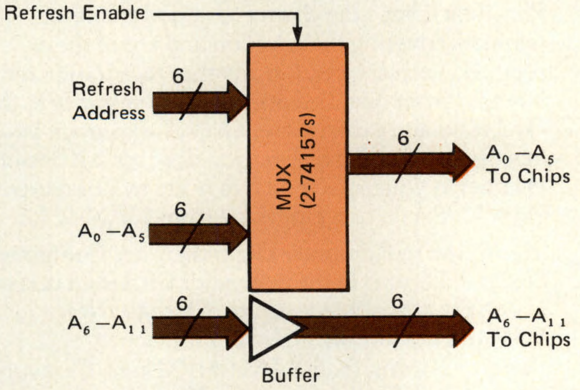
On the plus side, a 16-pin 4K RAM drives only 24 to 36 address inputs – half as many as an 18-pin device – and thus requires half as many address drivers, or two less ICs. With its fewer drivers, a 16-pin 4K RAM also generates half as much noise as an 18-pin unit. The reduced number of address lines means that a typical 16K x 18-bit board requires 288 in. less etch for address-multiplexing lines.

House next focuses on I/O. Because it multiplexes Data Out and Data In, an 18-pin part uses one I/O pin, one less than the non-multiplexed 16-pin part. Despite its greater pin economy, however, an 18-pin 4K RAM sometimes complicates timing, especially during a read/modify/write cycle. Before you can start such an operation on an 18-pin part, House explains, you must turn off the chip's Out driver, wait for its turn-off delay, turn on the chip's external Data In driver, then wait for the turn-on delay. Eighteen-pin 4K RAMs also require a three-state or open-drain driver to turn off the Data In driver.

Next, House analyzes the clocking capabilities of 18- and



ADDRESS MULTIPLEXING FOR 16-PIN 4K RAM



ADDRESS MULTIPLEXING FOR 18/22-PIN 4K RAM

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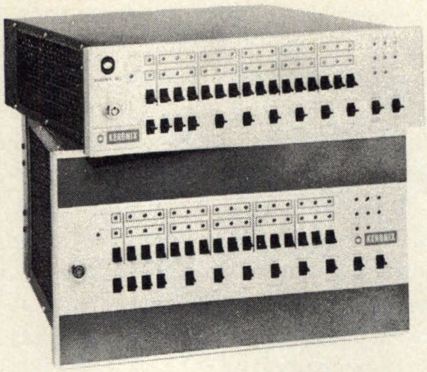

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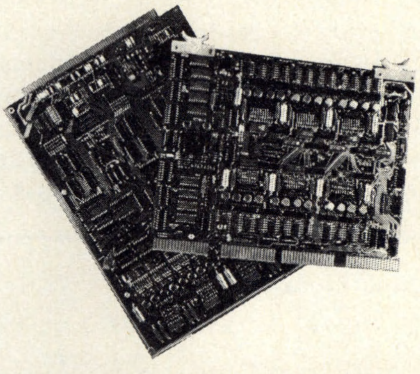

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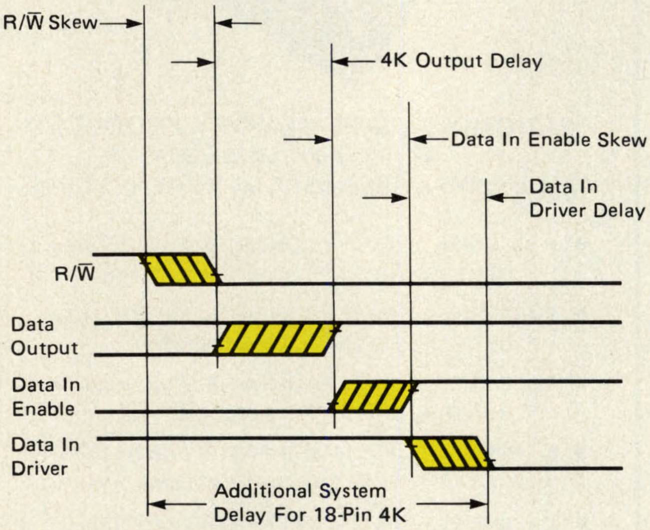
16-pin 4K RAMs. Sixteen-pin 4K RAMs provide both an on-chip TTL clock and voltage level shifter/amplifier that serves as an internal TTL-to-MOS converter, while 18-pin units require these devices in separate packages. Because they must sense $\overline{RAS}$'s leading edge and activate an internal timing generator and other circuits at the start of a memory cycle, the on-chip converters must maintain a constant standby current of about 1 mA. A 16-pin 4K RAM's chip drivers dissipate more dc power than an 18-pin part's MOS clock.



READ/MODIFY/WRITE CYCLE TIMING FOR MULTIPLEXED I/O

But off-chip drivers also dissipate dc power. Available as quad and dual devices, an 18-pin 4K RAM's off-chip drivers dissipate between 50 mW and 290 mW each. Because most drivers control between 8 and 16 chip enable pins, a typical 18-pin 4K part dissipates 3 mW to 18 mW. Moreover, disabled MOS-level clocks have low chip-enable input, and MOS-level drivers usually dissipate more power at low outputs. In an 18-pin RAM, therefore, the off-chip drivers dissipate more power in standby than in any other operating mode.

Because of its on-chip TTL-to-MOS conversion capability, a 16-pin part needs an extra 30 to 50 ns to activate its MOS-level clock. Eighteen-pin parts, however, create transmission-line delays of about 5 to 8 ns with distributed capacitance. Thus, in printed circuit boards with 17- to 33-pF chip-enable inputs, TTL-MOS converters increase system access times by 37 to 52 ns.

House also notes that 16-pin units use a push/pull output stage, while their 18-pin counterparts provide either open-drain or push/pull, three-state outputs. As a result, 16-pin 4K RAMs, which incorporate active pull-up devices and thereby cut impedance in the high state, are less sensitive to noise than 18-pin parts.

Sixteen- and 18-pin 4K RAMs also differ in another respect: the 16-pin parts incorporate output latches. Off-chip latches increase an 18-pin 4K RAM's access time by 17 to 30 ns and for a 16K x 16-bit storage card dissipate 17 to 19 mW for each 4K. The on-chip latches required by the 16-pin RAM, on the other hand, save more power than that device's TTL clock converters consume. Sixteen-pin parts, therefore, require less standby power than 18-pin units even if you discount the power consumed by the off-chip TTL or MOS clock drivers.

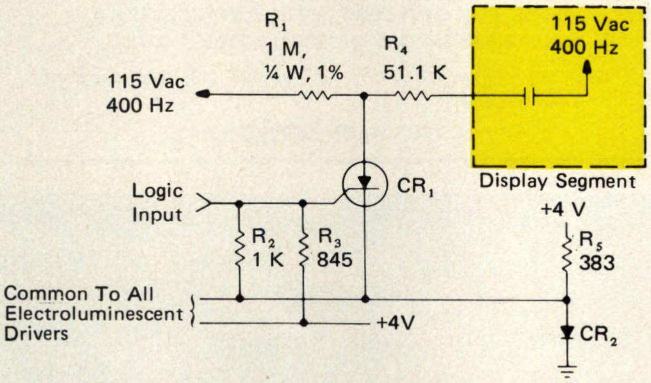
External latches, furthermore, force you to add separate packages to a 4K RAM to compensate for the absence of an output data latch on the chip itself. A typical 16K x 18-bit storage card requires 3 to 6 additional regular 16-pin packages.

Finally, House notes that 16K RAMs – which will eventually displace 4K units – require 14 non-multiplexed address inputs or seven multiplexed address inputs. Replacing a 16-pin 4K RAM's chip select (pin 13) with another address input results in the pin configuration of a 16-pin 16K RAM, with 1K/pin. Similarly, replacing the 22-pin 4K RAM's spare pin (pin 16) and its chip select (pin 5) with two more addresses gives you the 22-pin 16K RAM's configuration. This conversion from 4K to 16K is more difficult with an 18-pin 4K RAM, concludes House.

Drive circuit pulses electroluminescent displays

Considered by many experts as a potential CRT replacement in large-panel display applications, an electroluminescent panel incorporates a thin phosphor film that emits light when subjected to a very intense electric field. Continuous excitation quickly degrades the film, however, and so such an electroluminescent display requires a driving circuit that can operate it in a pulsed mode.

Designing such a circuit around electromechanical relays exacts penalties in power consumption, size and weight, notes C. B. Kirchen of Grumman Aerospace Corp. And, he adds, relays exhibit far higher failure rates than equivalent solid state devices. With these factors in mind, he designed an all-solid-state driver circuit around a silicon controlled switch (CR1) that conducts in both directions when subjected to an ac signal.



When the circuit's logic input – normally 4 Vdc – switches to zero, CR1 turns off and the driven electroluminescent display segment experiences 115 Vac (rms) at 400 Hz. Resistor R3 in the NASA-sponsored circuit sets the base drive current, while R4 limits that current if the display segment shorts out. Resistor R2 provides a reserve bias on CR1's base and prevents the segment's turning on when the high-voltage ac is applied but no logic power is present.

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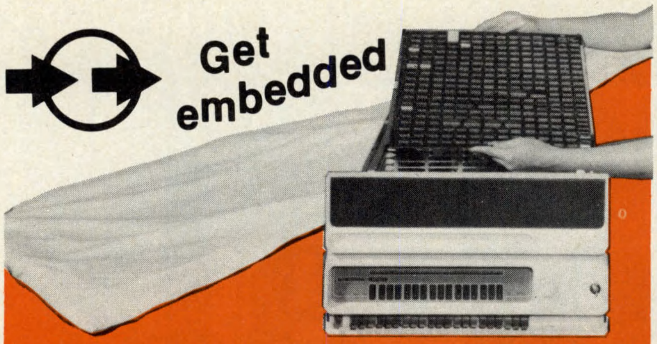

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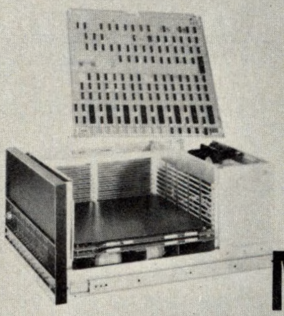

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CIRCLE 36

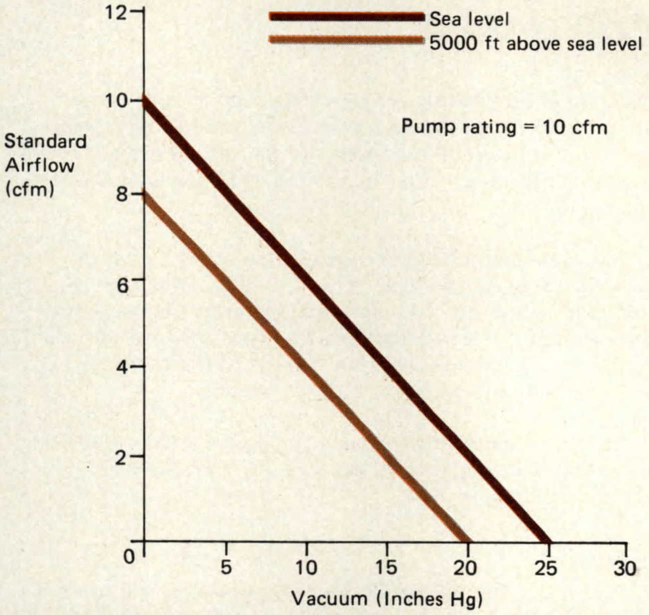
Vacuum-generation techniques for DP-equipment design

Mention "vacuum" and most digital-systems designers think of high-vacuum chambers, intricate tests and expensive equipment. But in many data-processing applications, inexpensively produced vacuums can lift, hold, feed or signal just as positive pressures can. They can pick up paper in high-speed paper handlers, buffer tape during sudden starts and stops and — applied through a tape drive's capstan slots — minimize tape wear and distortion. Positive air pressures, on the other hand, can maintain constant card heights or paper heights in card readers and paper handlers and separate sheets in handlers.

But for all their versatility, pressures and vacuums present some design difficulties as well, warns Eugene Brooks, director of engineering, Gast Manufacturing Corp., Benton Harbor, MI. For example, a vacuum-buffered tape drive that operates perfectly at sea level can fail at higher altitudes.

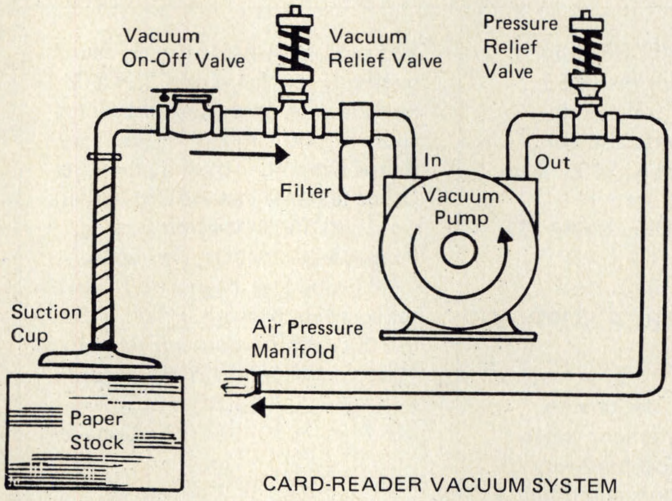
To understand why this problem occurs, assume that vacuum pump effectiveness refers to the percentage of atmosphere evacuated from a closed system. At sea level (barometric pressure 30" Hg), a pump with a 24"-Hg maximum vacuum capability thus produces an 80% vacuum. If your application requires pressure reductions to 25" Hg at sea level, this pump will probably prove adequate.

But suppose your design must also operate in Denver. Don't expect the same vacuum pump to continue to meet your requirements, Brooks warns. An 80% efficient pump that produces a 24"-Hg vacuum at sea level generates pressures of only about 20" Hg in the mile-high city, where the barometric pressure averages only about 25" Hg. So if your system requires a vacuum of 22" Hg at sea level, you should specify a pump that attains a maximum 27.5"-Hg vacuum if you want the system to operate in Denver as well.



In most data processing equipment, however, the airflow at some vacuum value less than the pump's maximum vacuum governs system operation. The accompanying graphs show how this flow varies with altitude for a 10-cfm pump that can attain 25" Hg maximum vacuum. At sea level, if this pump operates at 15" Hg, it generates a 4-cfm airflow. In Denver, however, the same pump generates only about 2 cfm. To provide a 4-cfm flow there, you'd need a pump with a sea-level airflow of about 12 cfm – at 5000 ft, such a pump would be about 80% efficient and would thus "look like" the 10-cfm unit does at sea level.

Consider several other factors when using a vacuum pump in data-processing-equipment design, advises Brooks. For example, install an intake filter between the pump and its relief valve. And check hoses, filter elements and valves if the vacuum gauge reads properly but the system doesn't work.



CARD-READER VACUUM SYSTEM

Many of the same accessories found on vacuum pumps should also accompany vacuum compressors. In all applications, install intake filters next to the intake port to prevent dirt from entering the compressor. But to ensure efficient operation, clean or replace filter elements as the level of contamination in the incoming air dictates.

Devices such as card readers often use both vacuum and pressure. To adapt a vacuum pump for such simultaneous operations without causing overloads, configure the system as shown in the figure. Instead of closing off the line, on-off valves should expose it to the atmosphere.

To avoid overloading the pump's motor or vanes, the combined vacuum load and pressure load should never exceed the pump's maximum continuous rating, says Brooks. A vacuum pump rated for a 20"-Hg vacuum continuous, for example, can simultaneously output a 10"-Hg vacuum and five psig pressure with no danger. As a general rule, in such applications reduce a pump's maximum recommended vacuum by 2" Hg for every psi of pressure on the pump's exhaust side.

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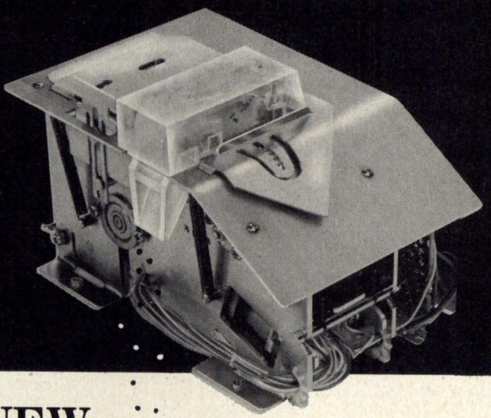

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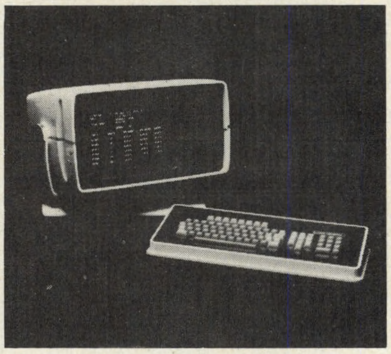
CIRCLE 37

product news

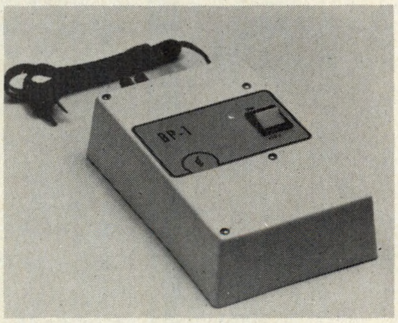
CRT TERMINALS SPORT DETACHABLE KEYBOARDS

For use as a system component with the manufacturer's minicomputers, this 1920-character (24 lines x 80 char.) video terminal comes in two versions, both of which incorporate a detachable keyboard and a monitor that swivels in two planes. The DG/Video Terminal 6053 provides direct cursor addressing and sensing, utilizes the 96-character ASCII set and incorporates an 11-key numeric pad, separate edit and cursor-positioning keys and 11 user-defined keys in addition to a standard typewriter keyboard. Additional character highlighting capabilities include blink, underscore and programmable intensity. The device communicates asynchronously at 10 switch-selectable speeds ranging to 19,200 baud and generates hardcopy output at 60 cps through an optional impact printer interface. The DG/Video Terminal 6052 utilizes the 64-character ASCII set, incorporates a keyboard with eight special-function keys and eliminates the higher-priced 6053's underscore and dual-intensity capabilities. You can obtain optional British, French, German and Swedish fonts for the 6053's 96-character set, and both terminals operate from any international power source. The units' detachable keyboards can mount up to 4 ft from their 12" CRT monitors. Prices: $2290 for the 6053, $1990 for the 6052, both in singles; quantity discounts available. Printer interface option: $400. Data General Corp., Southboro, MA 01772. (617) 485-9100 **Circle 201**



UNINTERRUPTIBLE SUPPLY OUTPUTS 5 VDC

For minicomputers, peripherals, alarms, portable equipment, emergency lighting, medical hardware, electronic cash registers and other OEM applications, this uninterruptible power supply incorporates a 2.8 Amp-hr lead-acid battery, a charging system and a 5V regulator and power inverter. Model BP-1/OEM outputs 5 Vdc at ±5% regulation and 9.1 Vdc from the battery, requires 115 Vdc @ 60Hz, recharges in six hours and operates over the -55° to 60°C range. Price: $140 in 1-9 quantities. Sunrise Electronics, 228 N. El Molino, Pasadena, CA 91101. (213) 963-8775 **Circle 202**

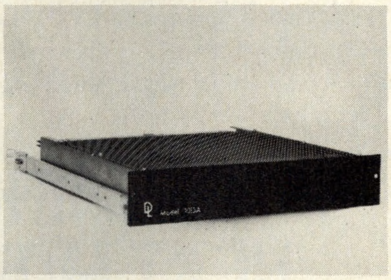


DISK CONTROLLER LINKS CALCOMP DRIVES TO INTERDATA MINIS

A single-card interface that serves up to four Calcomp Trident disk drives, this controller occupies one chassis slot in any Interdata minicomputer and incorporates a 512-byte RAM expandable in 256-byte increments to 2K. Sector buffering lets the Model TDC803 operate with or without a selector channel, and jumpers let you vary sector size in one-byte increments. Other features include CRC generation, rotational-position sensing, dual-access capability, on-board logic probe and diagnostic/formatter software package. Price: $1520 in 100s. MiniComputer Technology, 1901 Old Middlefield Way, Mountain View, CA 94043. (415) 965-4567 **Circle 284**

TAPE FORMATTER SERVES IEEE BUS

This buffered magnetic tape formatter lets you add any magnetic tape drive to the IEEE 488-1975 standard interface bus. Standard features include read-after-write error-checking with automatic correction and data retention during inter-record gaps. A dedicated Zilog Z-80 microprocessor oversees both the bus interface and memory management functions. Model 1015A's 7-track version records 200, 556 or 800 cpi in NRZI format. The 9-track models record 800 and 1600 cpi phase encoded. Available in 110 V or 220 V models, the rack-mountable formatter provides command functions that include set record size, write data to bus, write file mark, read data from bus, erase gap, input system status and edit mode. Dylon Corp., 7854 Ronson Rd., San Diego, CA 92111. **Circle 287**



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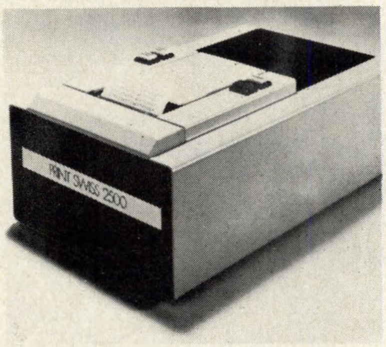
product news

16-COL. PRINTER OUTPUTS 2.8 LPS

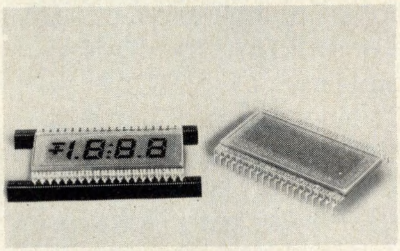
Utilizing a Seiko EP-101 printhead that outputs 16-character columns, this impact printer generates 2.8 lps and simultaneously accepts DTL/TTL-compatible BCD data for all columns. Print Swiss 2500's inputs include 21 lines for controlling decimal-point printing between columns. The unit can electronically control two-color printing and paper feed and can electrically select a standby mode that – without a print command – turns off the motor after five seconds. Measuring 9.5"W x 15"D x 6"H, the parallel printer requires 115 Vac @ 0.25A, accepts 3.5" paper rolls or fan-fold paper and incorporates a "paper-low" microswitch. Price: $925, including mating-input connectors, power cord and paper. Master Digital Corp., 1308-F Logan Ave., Costa Mesa, CA 92626.



Circle 282

FIELD EFFECT LCDS COME IN 5 HEIGHTS

Requiring 2.5 μW to 24 μW typical for all segments, these 3.5-, 4-, 4.5-, 5-, 6- and 8-digit 12-hr clock and 16-segment alphanumeric LCDs suit portable and battery powered devices, digital clocks and instrumentation. Available in five heights ranging from 0.4" to 1.0" and in reflective (for ambient lighting) or transmissive (for backlighting) models, the 0.120"-thick Polaris series is readable at up to 110°, offers a 20:1 contrast ratio and lasts 50,000 hrs at -20°C to 60°C. The displays' uniformly spaced integral contact clips solder to PC boards or insert into strip sockets on 0.100" centers. Prices for four-digit assemblies start at $10 in 100s. Industrial Electronic Engineers, Inc., 7720-40 Lemona Ave., Van Nuys, CA 91405. (213) 787-0311 **Circle 286**



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Printing 180 cps, this programmable interactive terminal communicates with any computer, thanks to a microprocessor that accommodates any existing protocol, code or mode. Model LX1010 can accommodate ASCII, BCD, Correspondence or other character sets and can transmit data synchronously or asynchronously at 75 to 4800 bps in full-duplex, half-duplex or echoplex modes. Other features include optional 140-cps printing, interchangeable 53-key alphanumeric and symbolic keyboard, 10-key cluster for choosing data-entry format and 12 prerecorded message keys. The unit also incorporates a nine-needle matrix printhead for information underscoring, italicizing and extended printing. LogAbax, U.S. Div., 10889 Wilshire Blvd., Los Angeles, CA 90024. (213) 477-0494 **Circle 290**

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This sampler contains 13 MOS/LSI interface circuits for computer peripheral equipment, along with technical data on each circuit. Devices include UARTs, a USRT, a baud-rate generator, keyboard encoders, a general interface controller, character generators and shift registers. Price: $99. SMC Microsystems, 35 Marcus Blvd., Hauppauge, NY 11787. (516) 273-3100

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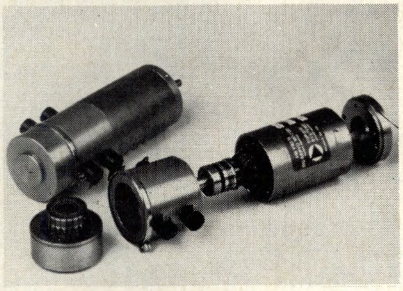

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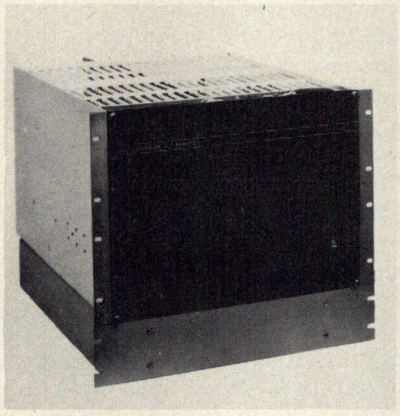

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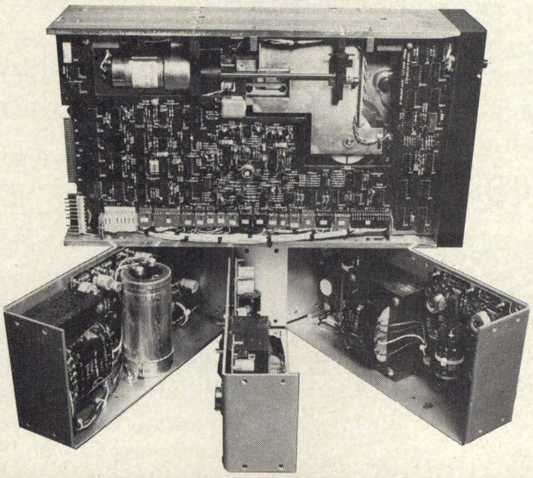

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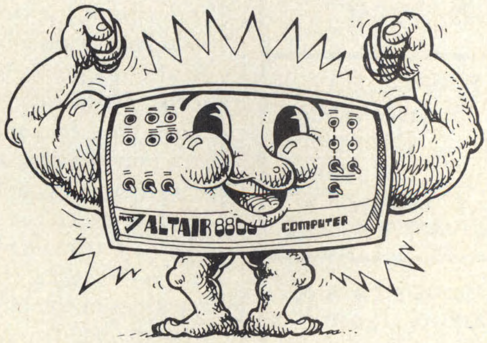

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product news

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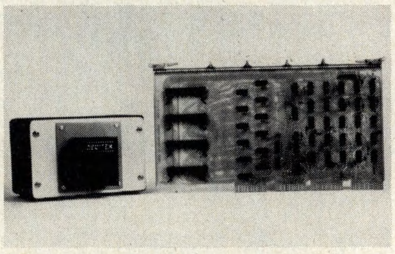
For DEC PDP-8/A computers, this paper-tape reader system interfaces DEC HSR codes through the manufacturer's eight-word interface — a combination that suits Model 400 to applications utilizing DEC writers instead of teletypewriters. Six additional words and flags remain on the interface for other data input requirements. Available in a stand-alone box or 19" rack-mount, the system incorporates a 150-cps Decitek Series 261 photoelectric head, power supply, cabinet and cable in addition to the interface. Forte Technology, Inc., 15 Strathmore Rd., Natick, MA 01760. (617) 655-5885 **Circle 283**



MULTI-FUNCTION KEYBD SPORTS 12 LIGHTED KEYS

For data entry, word processing and system automation, this 3 x 4 multi-function keyboard utilizes independently lighted keytops. When linked to a microprocessor system, the unit operates in "light on," "light off" or "blinking light" modes, each of which can represent a different system instruction or operator verification. The keyboard also operates in combinations of these modes. Standard features include translucent blank-white keytops, encoded output for calculator format, two-key rollover, n-key lockout and 5V incandescent lamps. Options include encoded output for telephone-type format, non-encoded output, incandescent lamps to 28V and customized keytop styling. Price: $69. Brynlaw Products, Inc., 1707 U.S. Hwy. 130 South, Burlington, NJ 08016. (609) 386-7733 **Circle 211**

ACQUISITION MODULE ACCEPTS CMOS INPUTS

For portable instrumentation, environmental data loggers and remote, battery powered microcomputer systems, this data acquisition module consumes 1.5W and sports 35-kHz throughput. Pin-compatible with the manufacturer's Datax II series, Model DT57C01 accepts both CMOS- and TTL-level inputs. The 12-bit module incorporates a 16-channel multiplexer, a buffer amplifier, a sample/hold amplifier and a 12-bit A/D converter, plus timing and control logic. It provides 12-bit resolution, ±½ LSB linearity, ±0.03% system accuracy, single-ended or differential input configuration and ±25ppm/^{0}C temperature coefficient. Price: $295 in singles, $175 in 100s. Data Translation, Inc., 23 Strathmore Rd., Natick, MA 01760. (617) 879-3595 **Circle 203**

ADD-IN MEMORY SERVES PDP-11s

Available in either 16K x 18 or 16K x 16 configurations on one PC board, this semiconductor add-in memory plugs into PDP-11 models 04, 05, 10, 34, 35, 40, 45, 50 and 55 computers. You can expand Add-in II's memory in 16K increments to 128K words and interleave its operation on 4K boundaries. Price for the 16K x 18 model: $1250. Fabri-Tek, Inc., 5901 County Rd. 18, Minneapolis, MN 55436. (612) 926-2721 **Circle 210**

FORMATTED TAPE DRIVE WRITES NRZI, PE FORMATS

Equipped with an interface that adapts it to most minicomputers, this formatted tape drive implements either NRZI or phase-encoded tape formats through circuitry on one 8" x 16" circuit board. It also lets you add up to three additional drives in a master/slave configuration. Operating at 12.5 to 75 ips and writing 800 to 1600 bpi, Model FT7000 provides file-search capability, space-record commands and a crystal oscillator for timing. Price: $3275 for PE version in OEM quantities. PCC/Pertec, 9600 Irondale Ave., Chatsworth, CA 91311. (213) 882-0030 **Circle 206**

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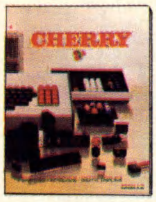

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ia7301 Compute
Programming P

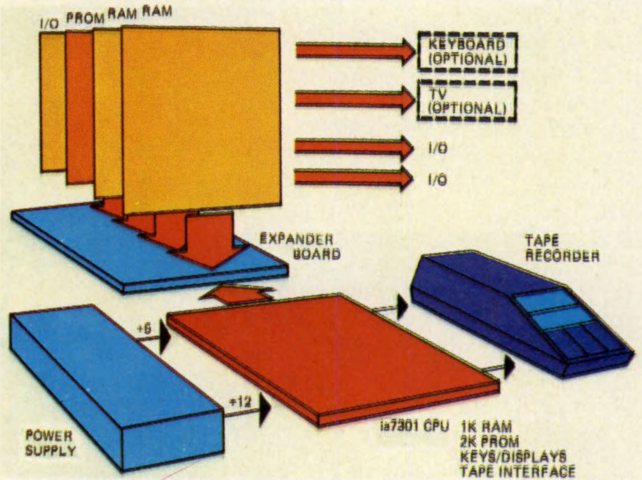
The fact is that right now microcomputer programming is a bear. Microprocessors are loaded with subtleties which make software development a long, arduous process. That's why we developed the ia7301 Computer in a Book.* It's a fully operational microcomputer system and a 250 page programming course all contained in a 3-ring binder. This is not a kit or a toy but a powerful, microcomputer system (based on the industry standard, the 8080) and a practical programming course specifically designed to quickly bring you up to a high level of understanding and proficiency in programming 8080 based microcomputer systems.

The Computer in a Book comes to you completely assembled and tested. All you need is an inexpensive dual voltage (+12V & +5V) power supply. The −5V is generated internally in the computer. There is nothing else to buy.

A super programming course

The programming course text is easy to follow and begins with a one instruction program to determine if a switch is open or closed. This is built upon and expanded through all 78 instructions until 250 pages later, you become adept at programming complex problems like multi-byte arithmetic and games of skill like Pong.™ Only with Iasis Computer in a Book can you have the advantages of a handy programming text together with an operational computer to load and test programs each step of the way and thereby learn the intricacies of microcomputer programming at a comfortable pace.

And since this microcomputer has a special built in monitor program which allows you to look into the operational parts of the system you'll never get bogged down in debugging or editing. The ia7301 Computer in a Book is the fastest way to learn everything about microcomputer programming.



Some great microcomputer features, too

The microcomputer system features a 24 pad keyboard, 8 seven segment LED readouts that display information in hexadecimal code which is far more versatile and advanced than binary or octal coded systems, and an onboard cassette tape interface for saving programs. The hexadecimal keyboard also contains 6 special mode keys which allow you to call up and change any data or instructions in the CPU registers or in the system's RAM memory. Likewise programs can be executed instantly or they can be stepped through one instruction at a time using the appropriate mode key, so that you learn your way around the inner working of an entire microcomputer system.

Also the write tape and read tape mode keys have been carefully designed for accurate and convenient operation with any home cassette tape recorder that has an earphone and remote microphone jack. Two LED indicator lamps tell how long it takes to dump or reload programs from the system's memory onto tape and back again. But in the reloading cycle, if any errors have occurred such as a lost piece of data or the volume knob is too low, the readout displays will indicate errors. This little feature prevents untold problems in debugging a reloaded program.

Upwards expandability from the start

We designed the Computer in a Book to be upwards expandable and not become a kluge in the process. The microcomputer contains 1K bytes of RAM memory, 1K bytes of PROM memory (containing the monitor program), and 2 I/O ports. The Computer in a Book is expandable to virtually any level you want, i.e. up to 65K bytes of memory and 256 I/O ports.

Optional expander boards are available and attach to the ia7301 computer at the top edge connector. A wide variety of standard interface boards can be plugged into the system to give add on memory, TV and teletype interface, and much more.

Thus what served as an educational system can now be upgraded for many new applications. We've included a machine language coding pad for writing and documenting programs, working out subroutines and pro-

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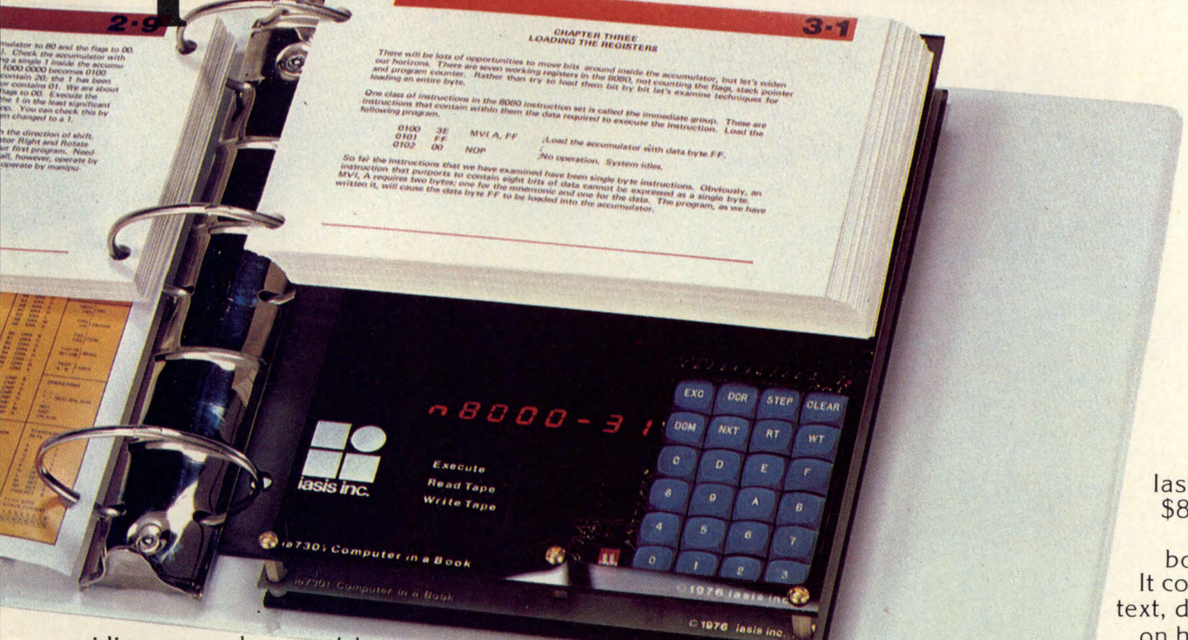
*U.S. Patent Pending
Pong is a trademark of Atari, Inc.

gramming is a snap
mputer in a Book



viding general support to a development system when extensive programming or debugging is necessary. The Computer in a Book may also be used to train field service technicians by putting verbal information and programs on cassette tapes. We are coming out with preprogrammed PROMs and extension tapes containing new application packages such as floating point arithmetic and micro-assembler programs. Our goal is simple. We want to provide microcomputers that are useful and practical.

A college assistance program

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Educators interested in exposing their students to a comprehensive background in Microcomputer programming should look into the Iasis Microcomputer Instructional Courses for their college or university. Send for our free pamphlet which describes ways of setting up short microcomputer programming courses. It offers some advice on structuring a coordinated and comprehensive program, so your students can learn programming and get valuable hands-on experience with operational systems at very reasonable prices.

The price

The complete Computer in a Book which includes an operational 8080 based system, 250 page programming course, machine code pad, hexadecimal conversion card all in a 3-ring binder is offered for only $450. The Computer in a Book has a 90 day parts and service warranty. Iasis also provides a check out list and start up instructions with each system. Please allow 30 days for delivery.

A free bonus

If you order your Computer in a Book before March 15, 1977, Iasis will give you an $8.00 Microcomputer Applications Handbook as a free bonus. It contains 144 pages of text, diagrams, and tables on hardware design and microcomputer applications. Order today. If the Computer in a Book isn't everything we say it is, then return it within 15 days for a full refund and keep the Applications Handbook as a gift. We're sure you'll find that microcomputer programming is a snap with the ia7301 Computer in a Book.

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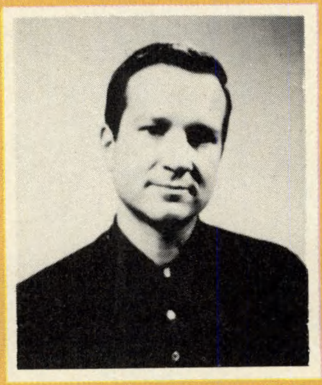

Innovative design: short-term sacrifice, long-term gains

Editor's note: "Beware of Micro Madness," the July Viewpoint by Edward Claggett, stated that practicing electrical engineering frequently means discarding old techniques and replacing them with new expertise, and that microprocessor-system design, the latest such design-method revamp, can often become mere "tinkering." Cautiously estimate the cost and performance benefits of using a microprocessor in your design, Claggett argued; proceed only if your development budget can support the required design efforts. Herewith, one reader's response to those ideas.

Acquiring new techniques need not render a designer's previous expertise obsolescent. Although an engineer may not have to understand vacuum tubes to get a job today, engineers who have such an understanding can solve a wider range of problems than those who deal only with solid state devices.

Designers often tend to define projects in terms of short-term objectives. But regarding such objectives as the only relevant ones can hamper a design effort.

Will the possible cost and scheduling overruns caused by some microprocessor-system design projects really prove damaging in the long term? Not really, for if a microprocessor application is truly novel, its potential advantages outweigh any problems caused by such short-term overruns. We'd make few advances if we analyzed every project on the basis of economics alone; indeed, the U.S.'s lead in high technology is eroding because many companies have failed to allocate enough funds to finance the research and development of new-product applications.

Engineers must innovate. If to innovate they must attend special programming courses or experiment with microprocessor design techniques, so be it. Such activities aren't "tinkering;" they have definite objectives and require finite amounts of time.

Before the microprocessor attains its full potential, innovative companies must make long-term commitments to encourage the new techniques that microprocessor-system design requires and to disseminate the knowledge that arises from applying those techniques. Relatively self-centered since its birth and currently conservative toward new-technology commitments, the computer industry must change its ways. The companies willing to foster innovation, and the engineers able to achieve it, will profit both materially and professionally.

Michael Hordeski

Michael Hordeski *is a Professional Engineer and president of Siltran Digital, Silverado, CA. We will be pleased to provide space for opposing views.*

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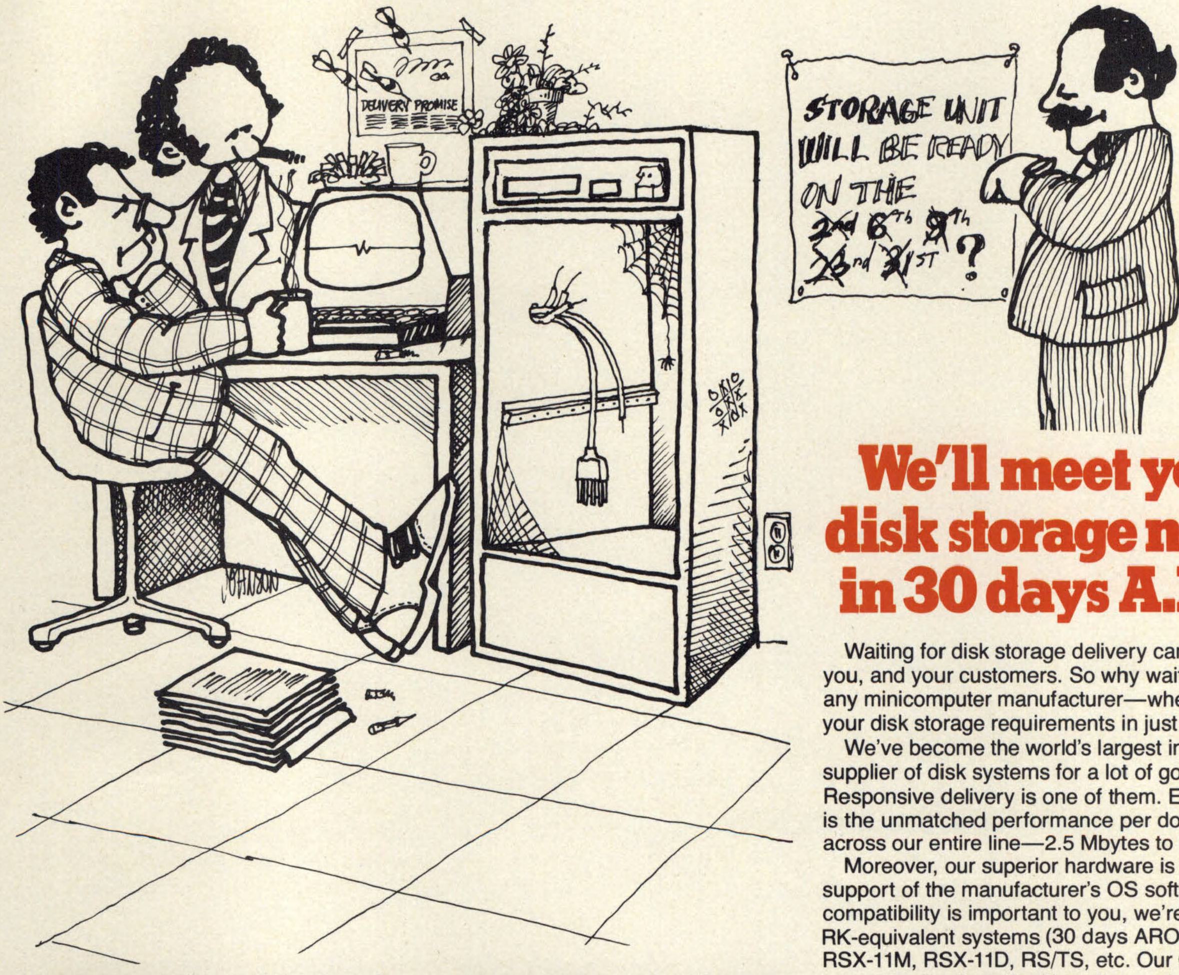
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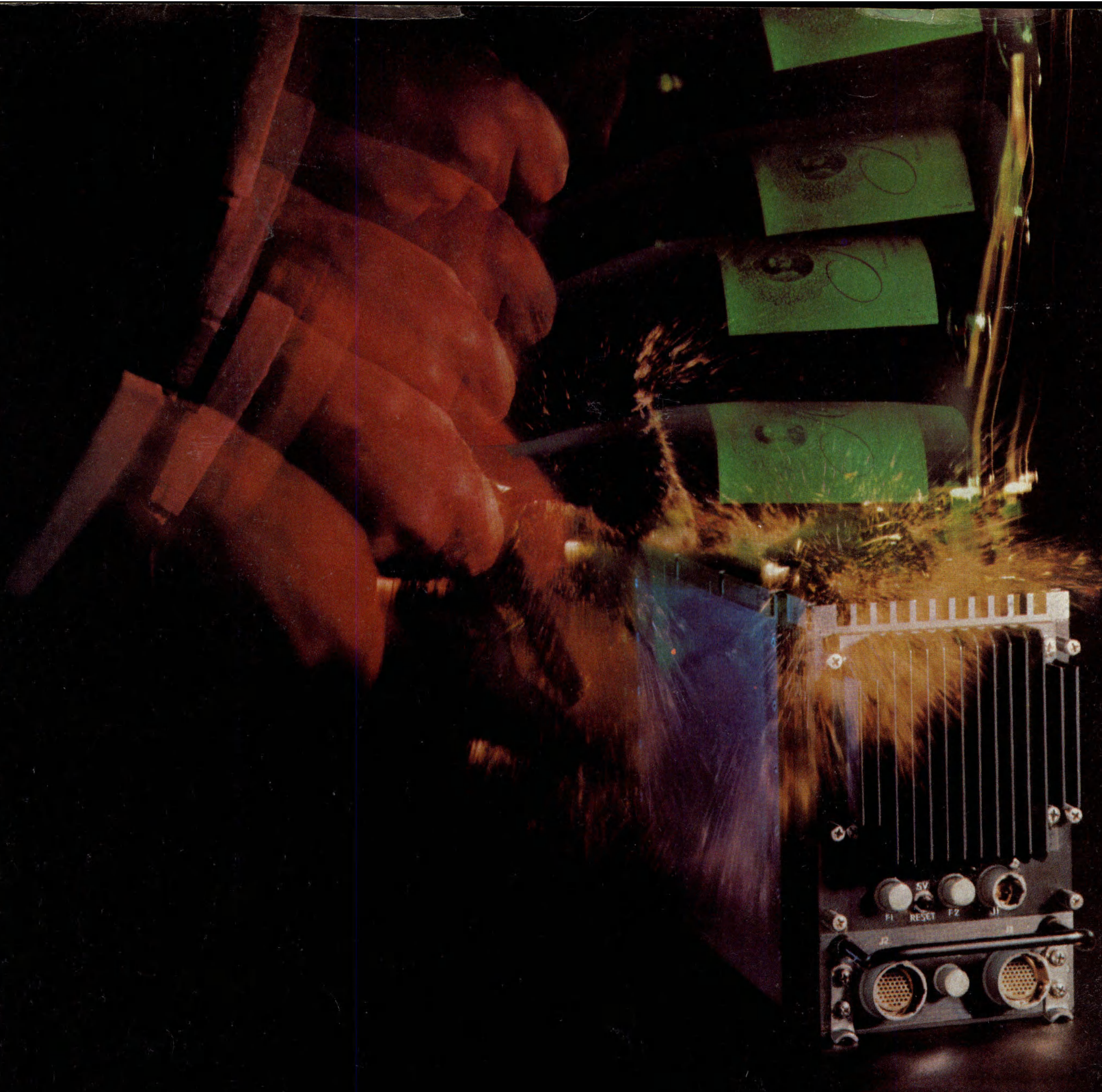

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